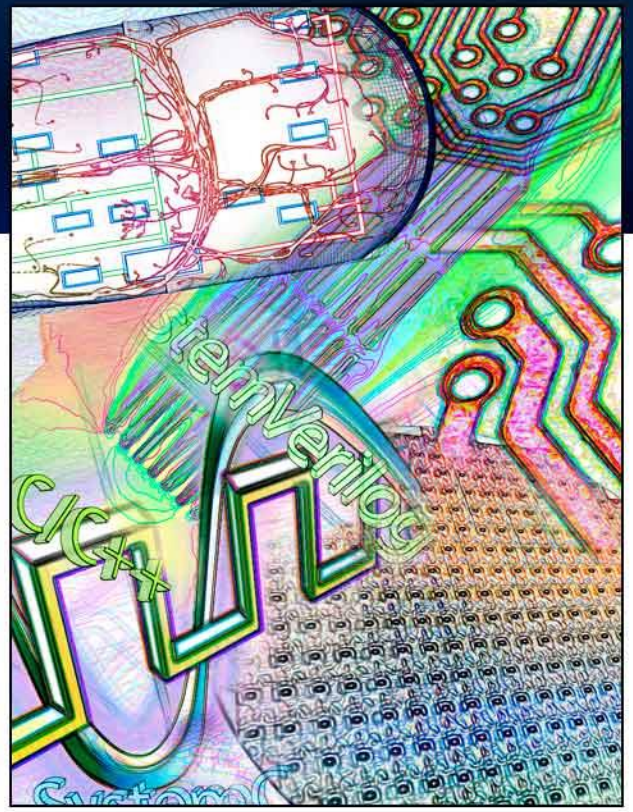
# Industry Pulse:

## *Trends in Functional Verification*



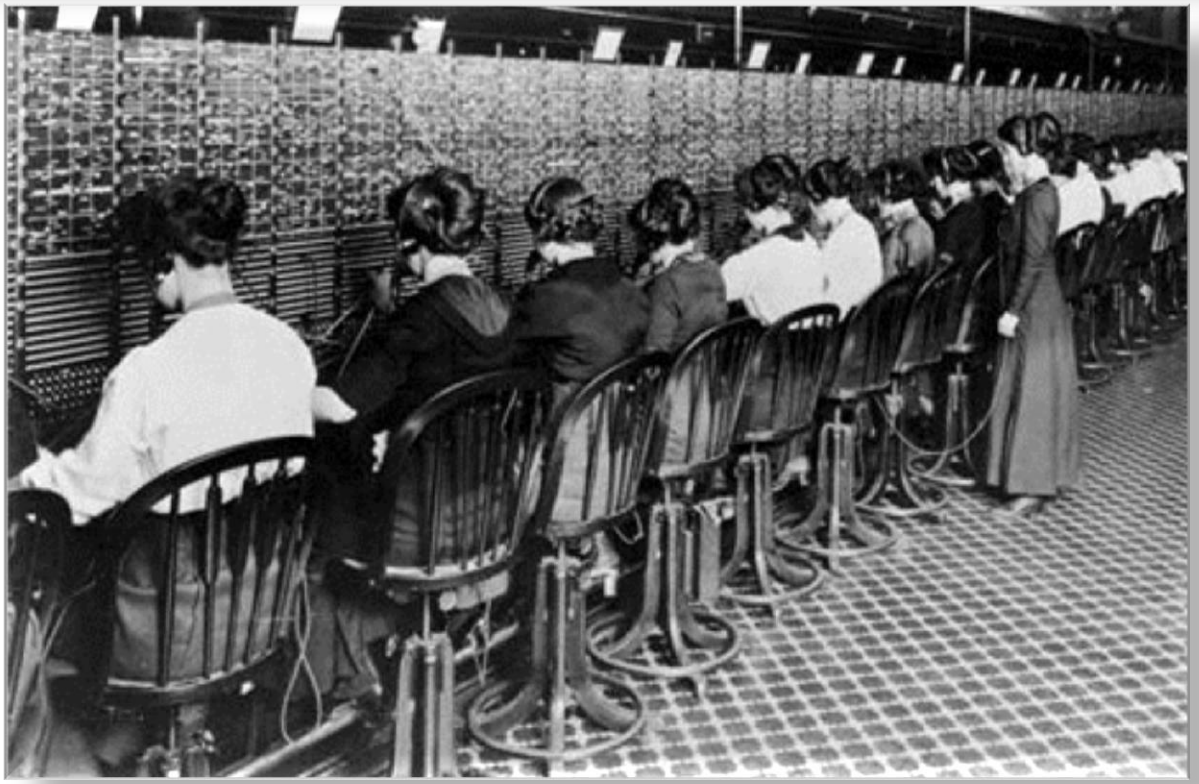

Harry Foster
Chief Scientist Verification
Design Verification Technology

*Memo*CODE 2013

Mentor Graphics®

# Extrapolating From Current Conditions Disregards Future Innovation

"In 1910, in the early history telephony, a Bell telephone statistician projected a massive ramp-up in switchboard operator jobs as telephone use grew, until "every woman in America" would be required."

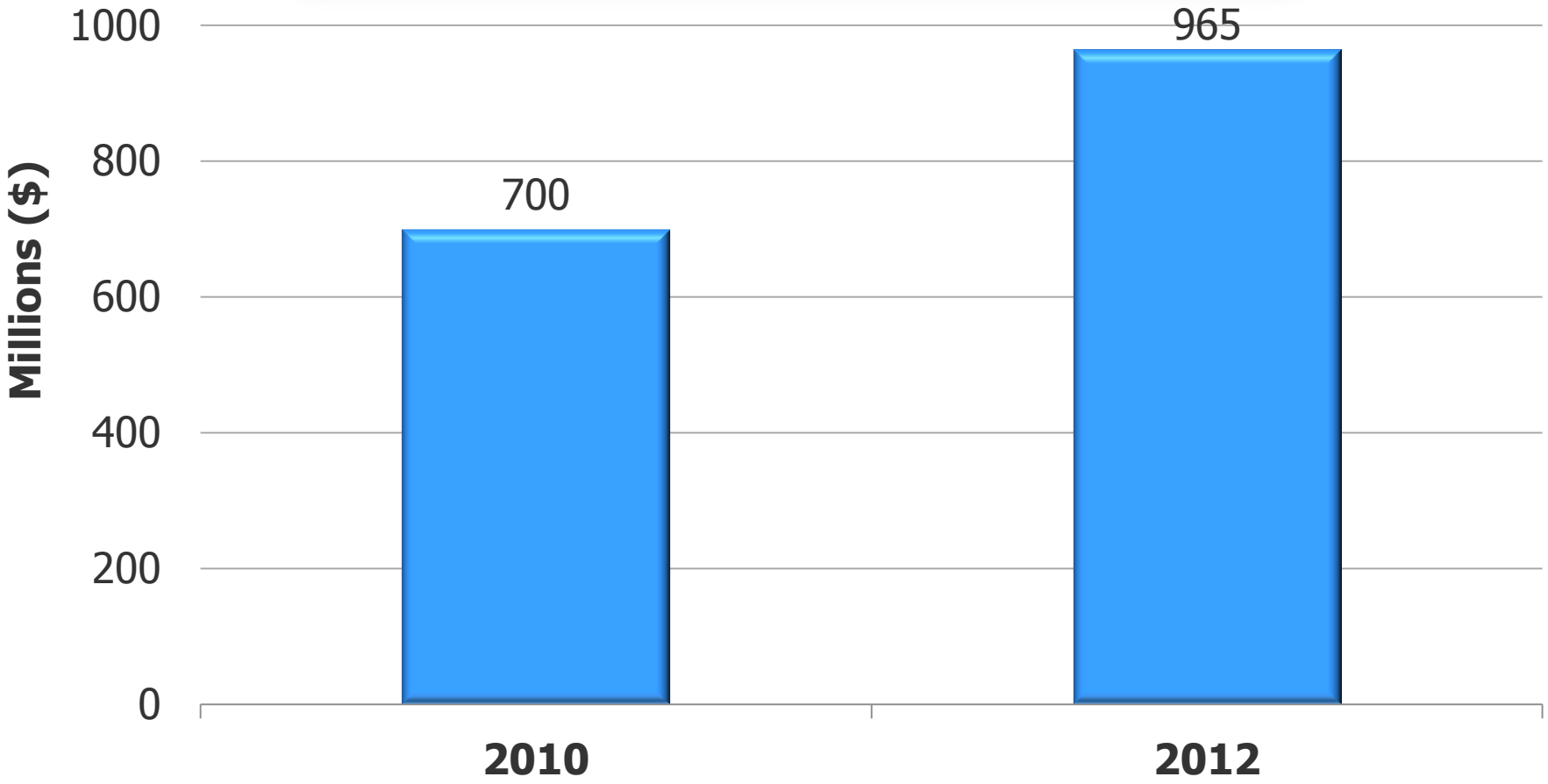


Source: Future Savvy: Identifying trends to Make Better Decisions, Manage Uncertainty, and Profit From Change Adam Gordon, 2008

# Functional Verification Market

*According to EDAC*

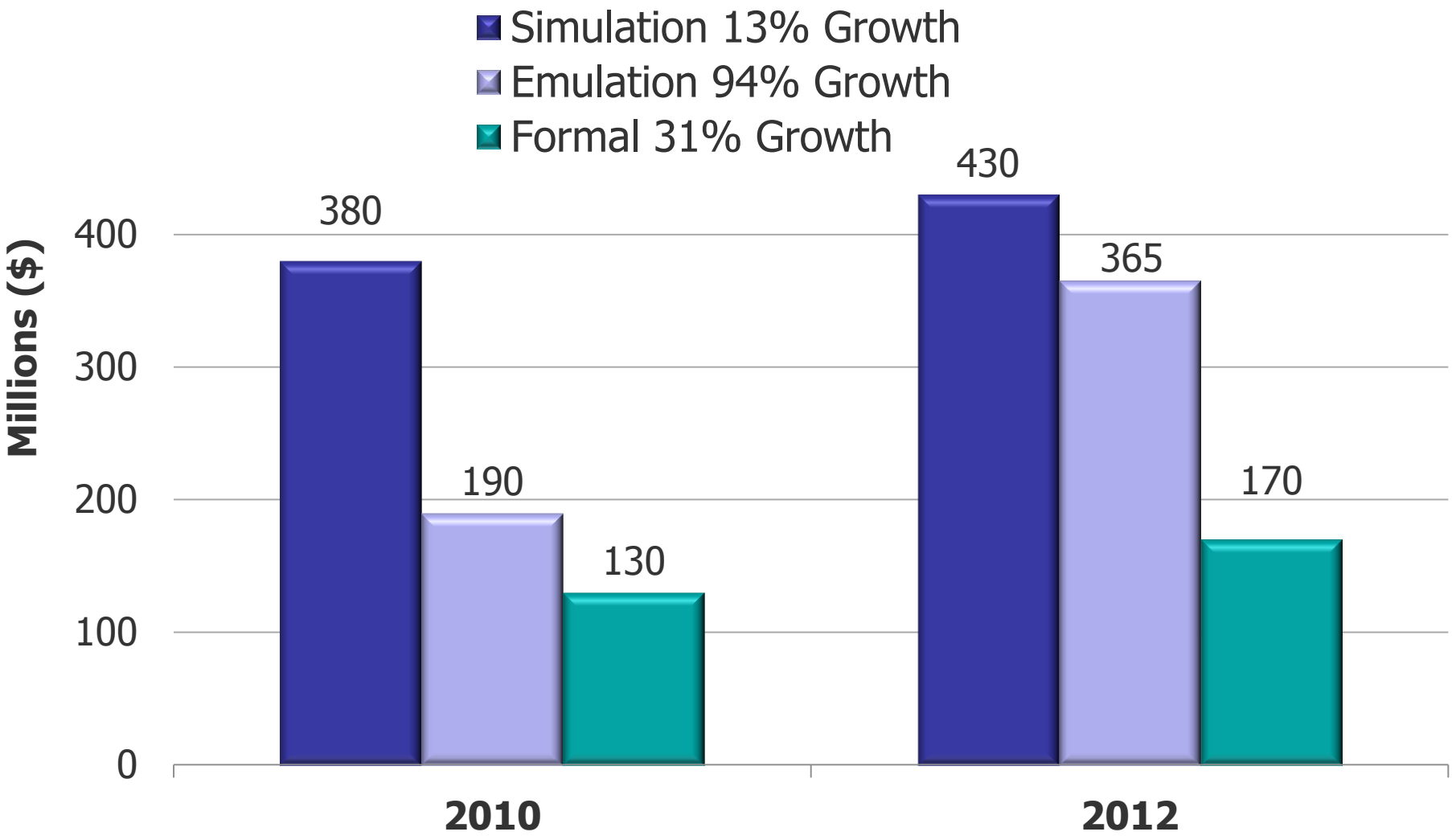
**38% Growth Between 2010 2012**




EDAC: Market Statistics Service 2007 Annual Summary Report

# Functional Verification Market

*According to EDAC*




EDAC: Market Statistics Service 2007 Annual Summary Report

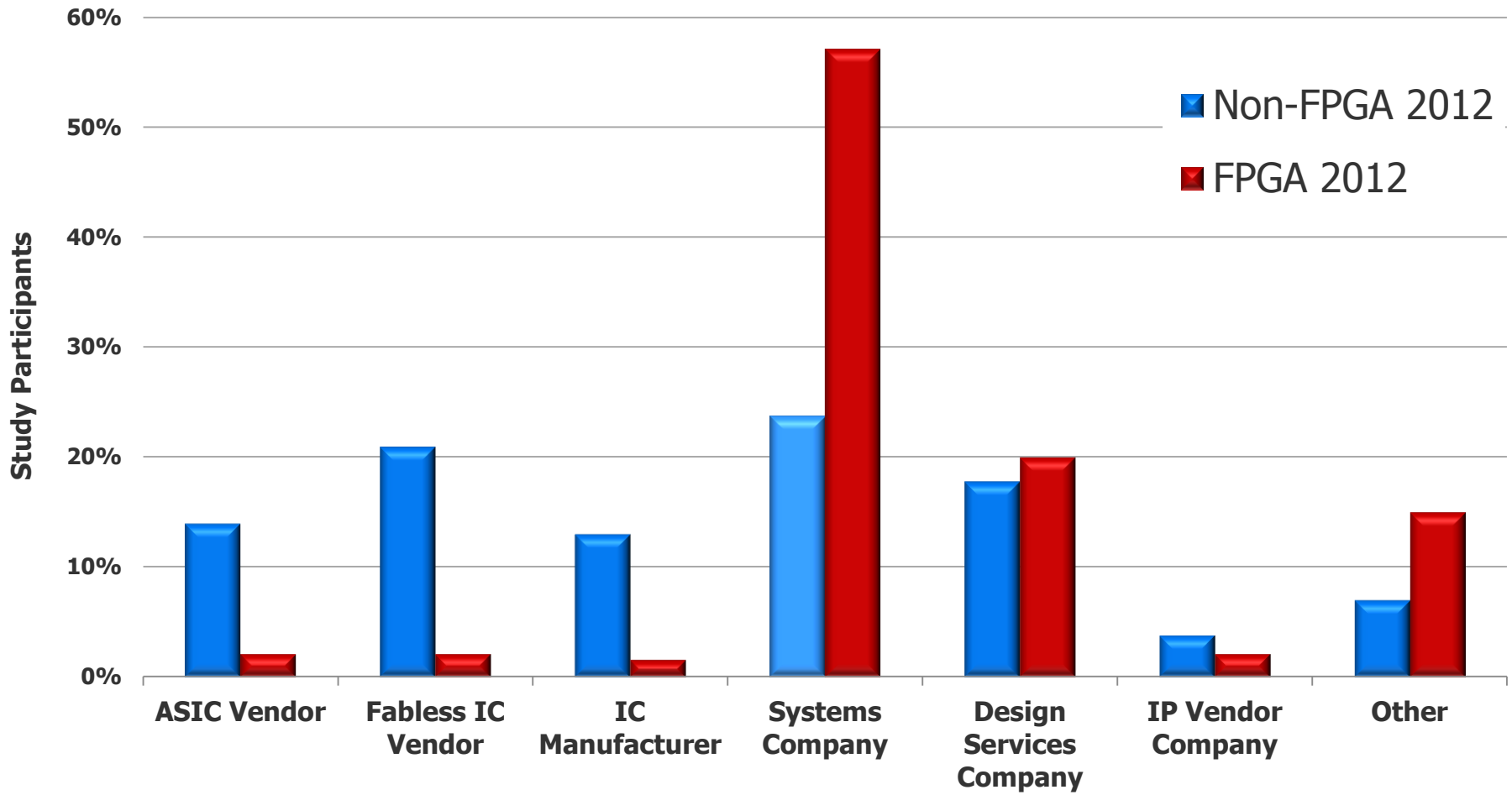
# 2012 Wilson Research Group

*Functional Verification Study*

- Conducted by Wilson Research Group
  - Commissioned by Mentor Graphics
  - Format followed 2002, 2004 Collett studies for trend analysis, as well as the 2007 FarWest Research Study
- Worldwide study
  - Overall confidence of 95% plus/minus 4.05%
- This was a blind study!
  - To eliminate any bias in the results
- This was a balanced study!
  - No single vendor dominated responses

# Who Participated In The Survey

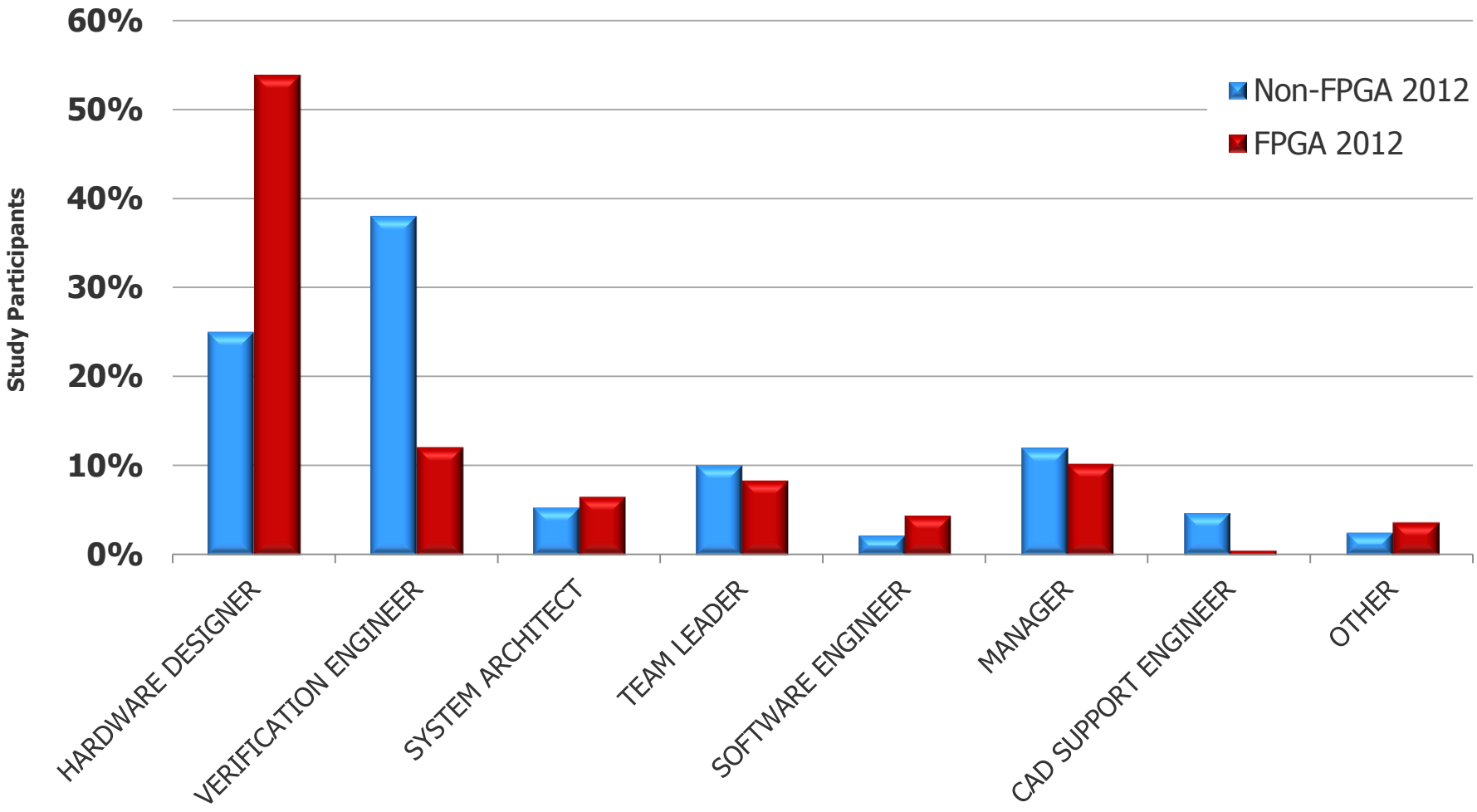
*Participant's market segment*




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Who Participated In The Survey

*Participant's job title*




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Overview

- Beyond Theory
- Beyond Standards
- Beyond the Status Quo

Beyond Theory in Terms of Rising Complexity

# BEYOND THEORY

# Difference Between Theory and Practice

In theory there is no difference between theory and practice, but in practice there is.

# Difference Between Theory and Practice

Theory: Everything is clear, but nothing works.

# Difference Between Theory and Practice

Practice: Everything works, but nothing is clear.

# Difference Between Theory and Practice

The problem is sometimes theory meets practice:

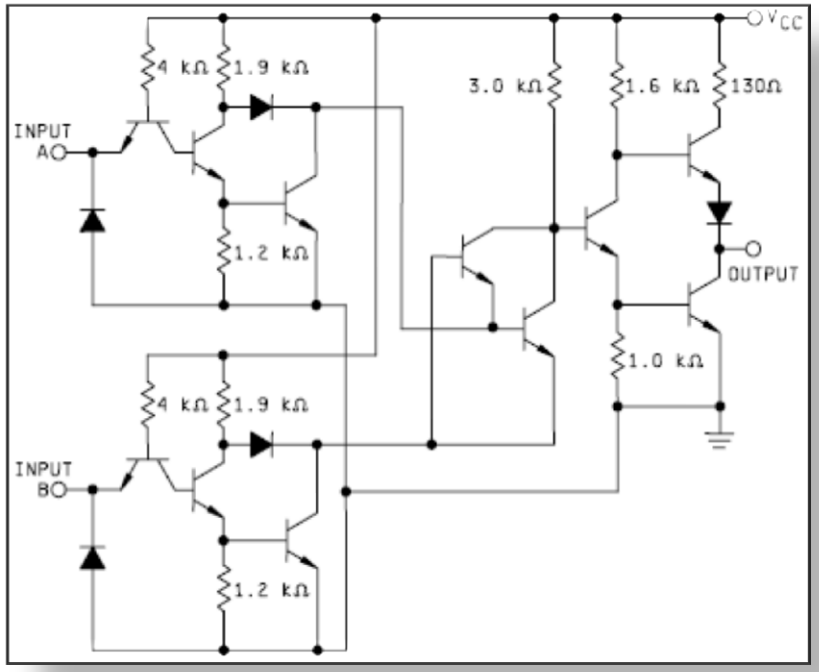
Nothing works and nothing is clear.

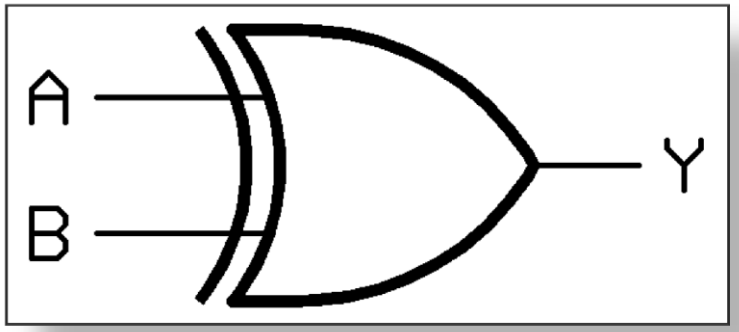
# Beyond Theory in Terms of Rising Complexity

- What does this really mean?
- What makes things complex?
- How do we measure complexity?

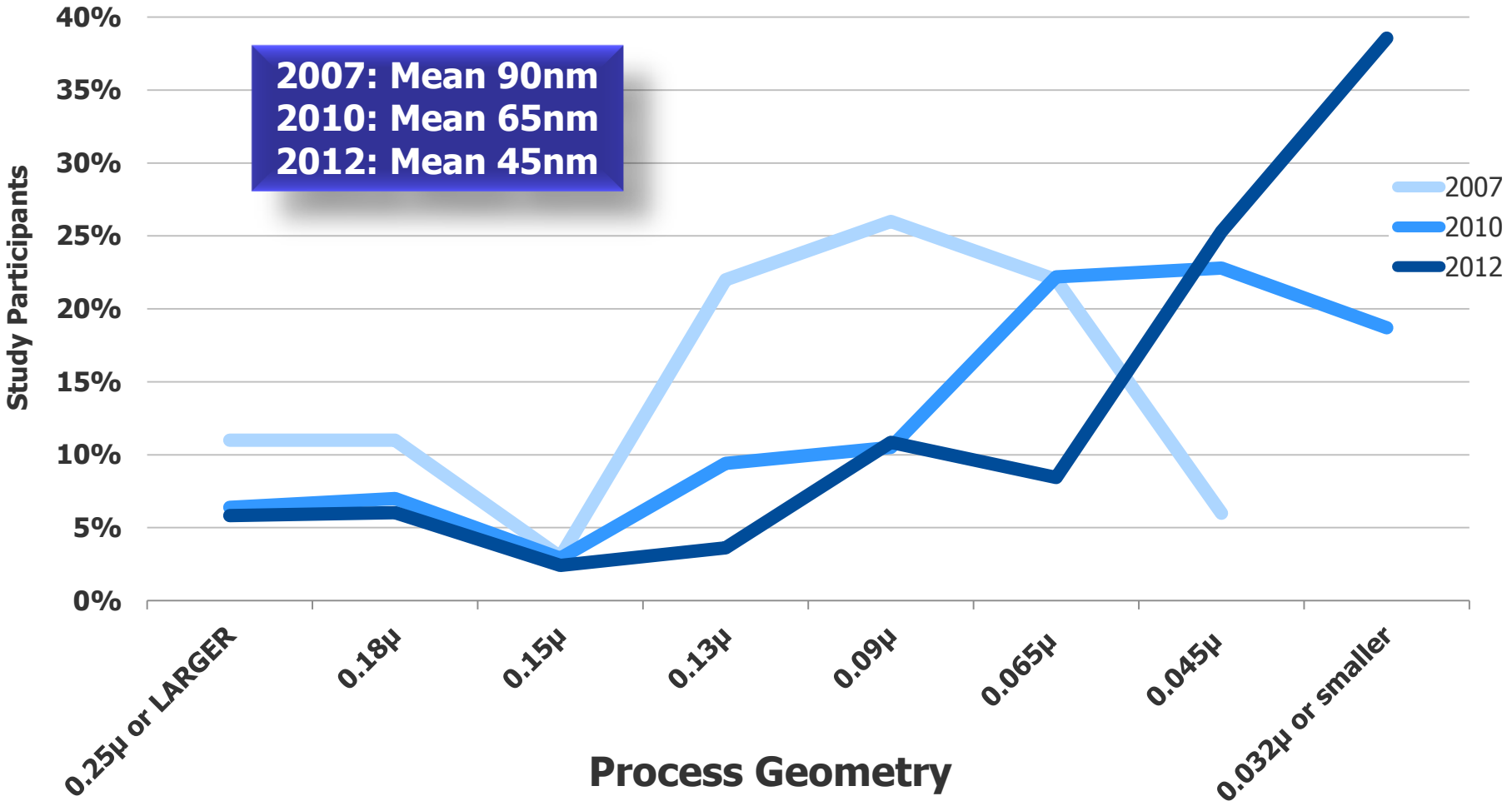
# What Makes Something Complex?

- System consisting of many interconnected parts
  - — Examining the individual parts tells you nothing about the system
- Complex does not necessarily mean complicated



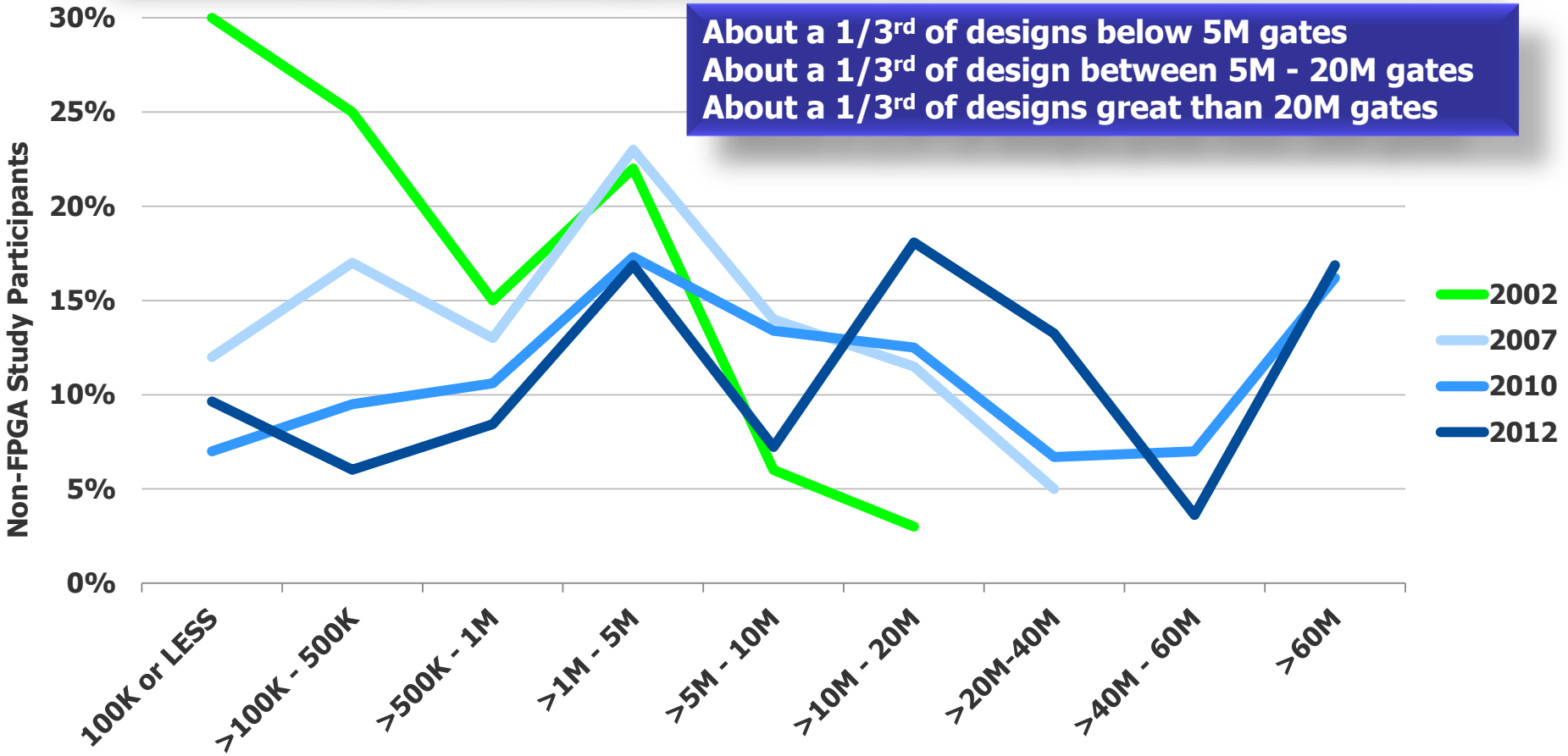
# Designs are Getting More Complex




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Designs are Getting More Complex

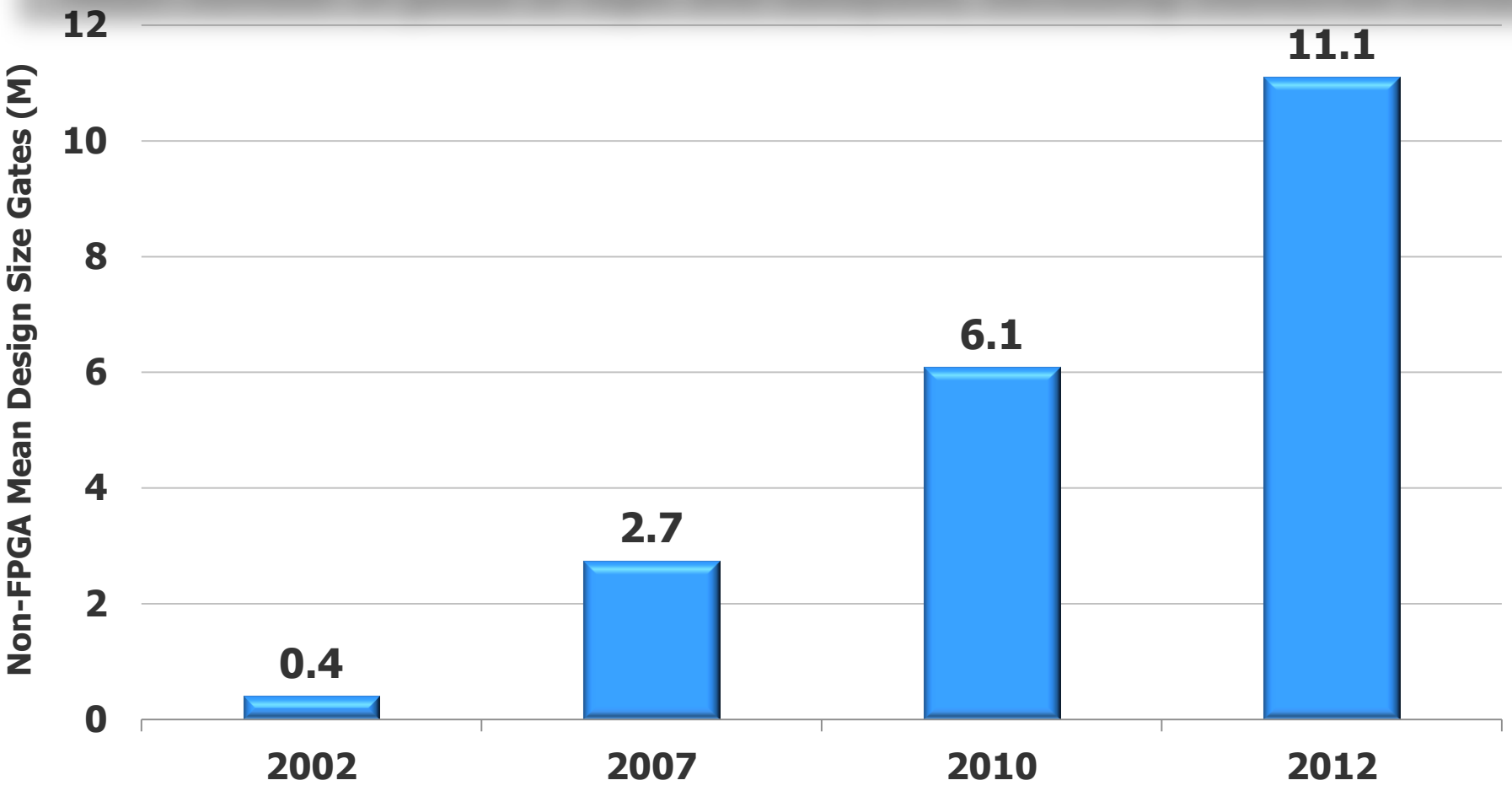
***Number of gates of logic and datapath, excluding memories***




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Designs are Getting More Complex

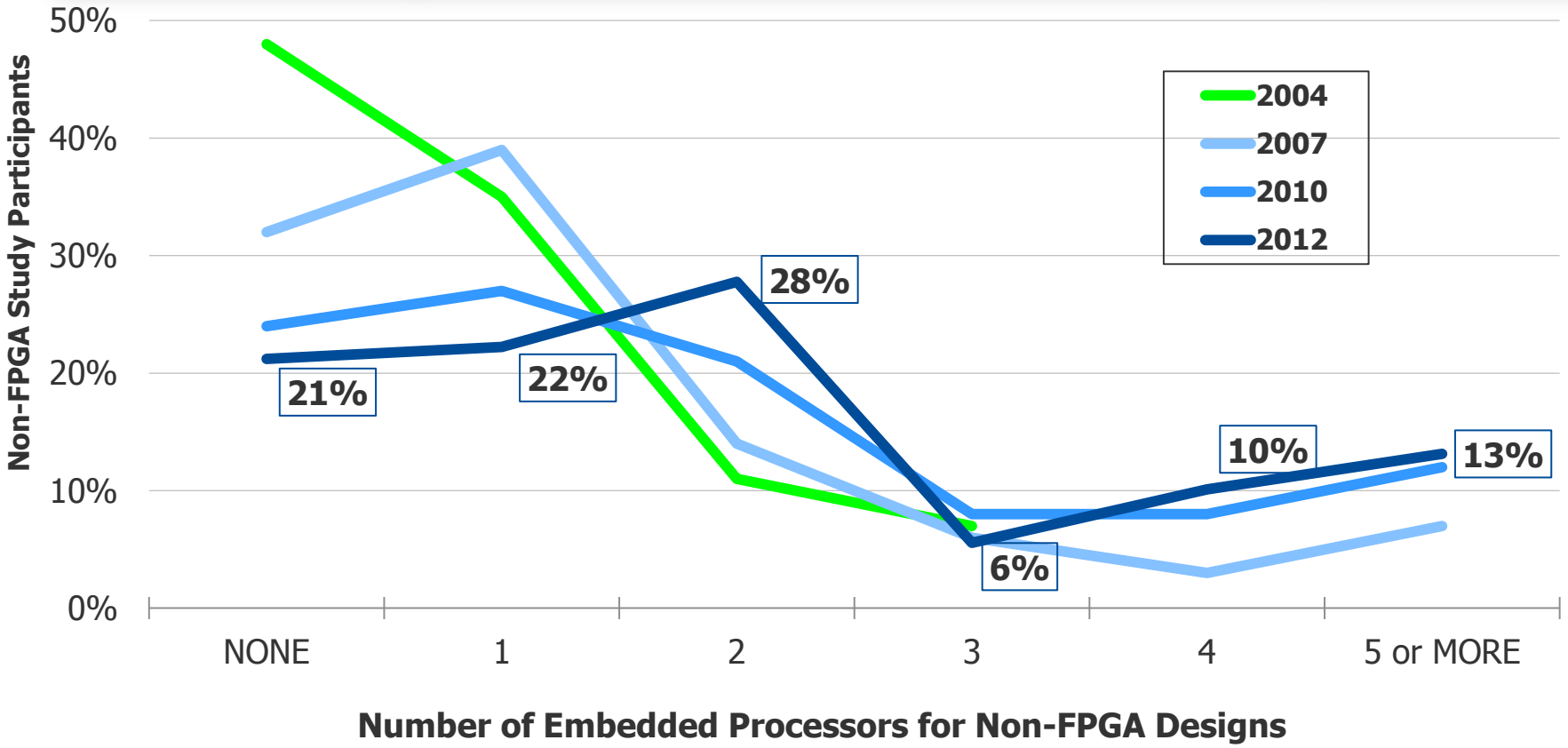
***Mean number of gates of logic and datapath, excluding memories trends***




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Designs are Getting More Complex

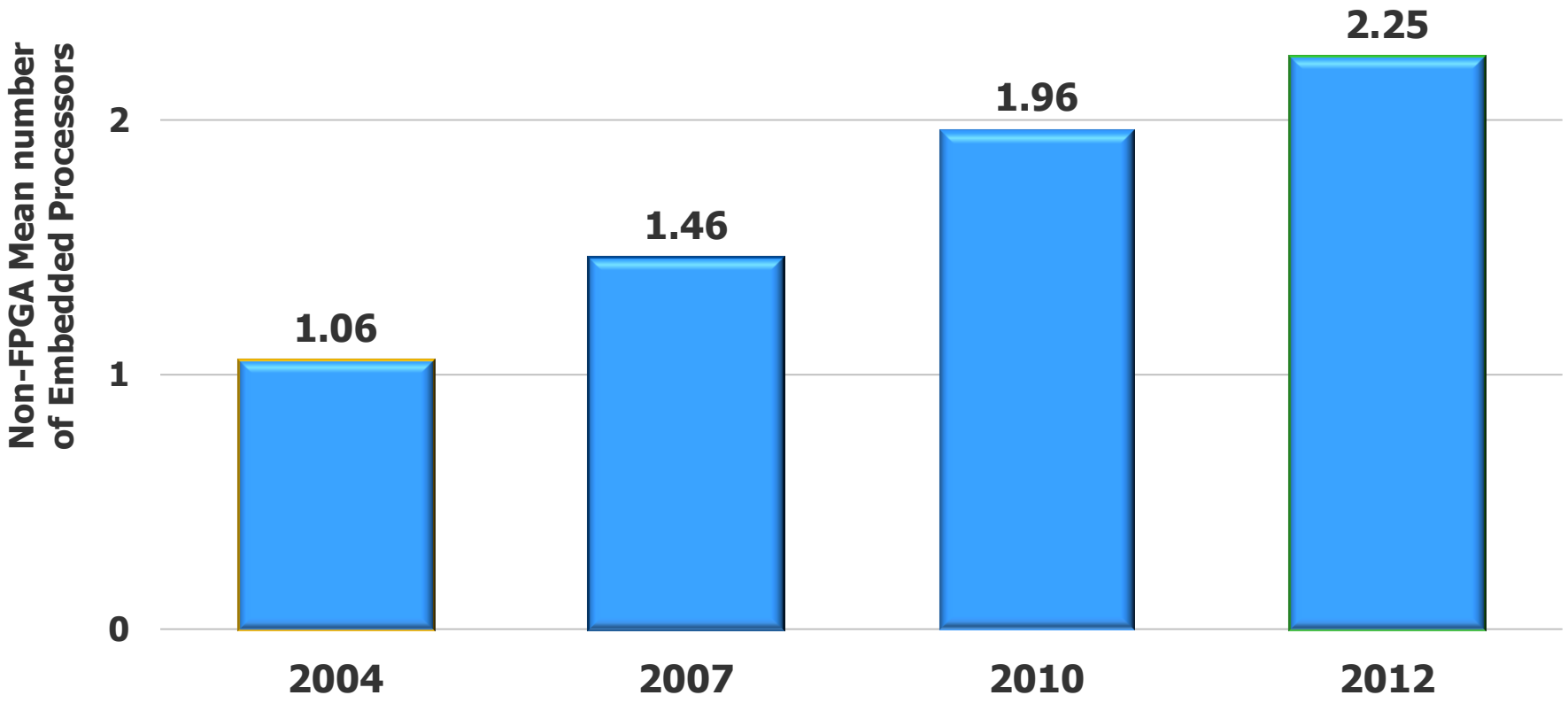
*79% of designs contain one or more embedded processors*




*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# Designs are Getting More Complex

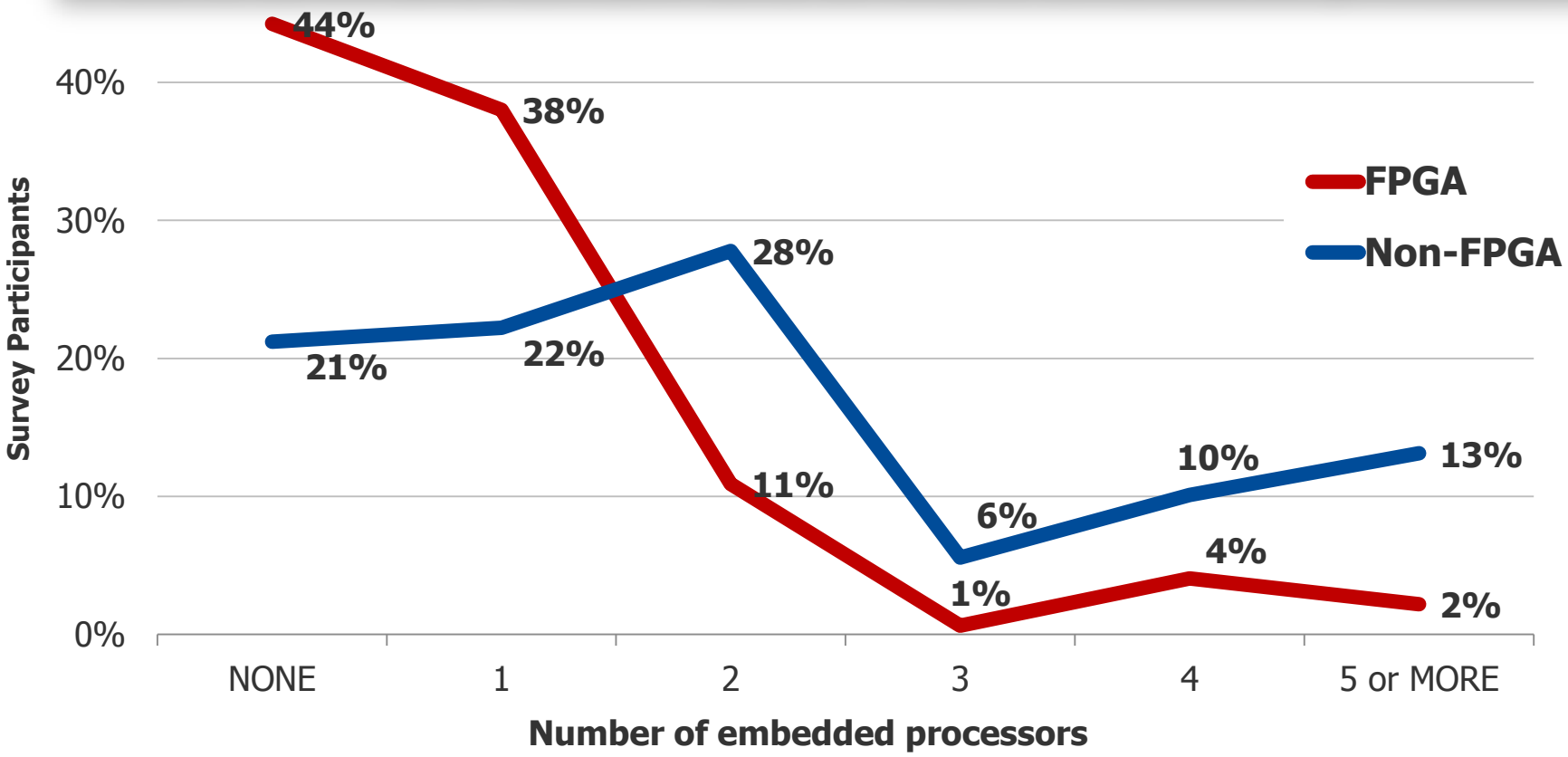
*Mean number of embedded processors continues to rise*




*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# FPGAs are Getting Complex Too!

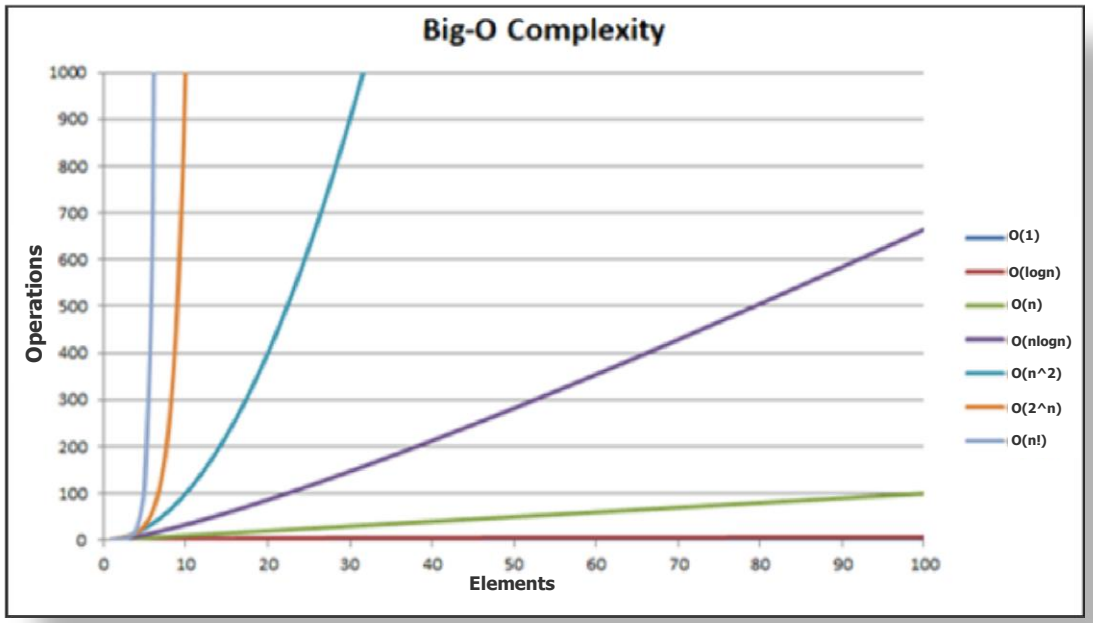
*56% of FPGAs contain one or more embedded processors*




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

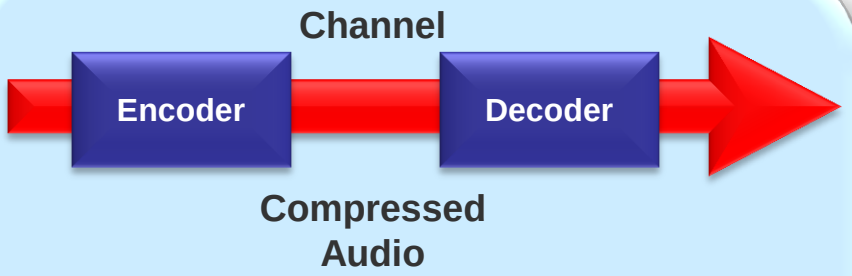
# How do we measure complexity?

- Computational complexity theory used in computer science




- There are no generally accepted metrics!

# Is bug density a good proxy?




- Single, sequential data streams
  - Floating point unit
  - Graphics shading unit
  - DSP convolution unit
  - MPEG decode
  - . . .

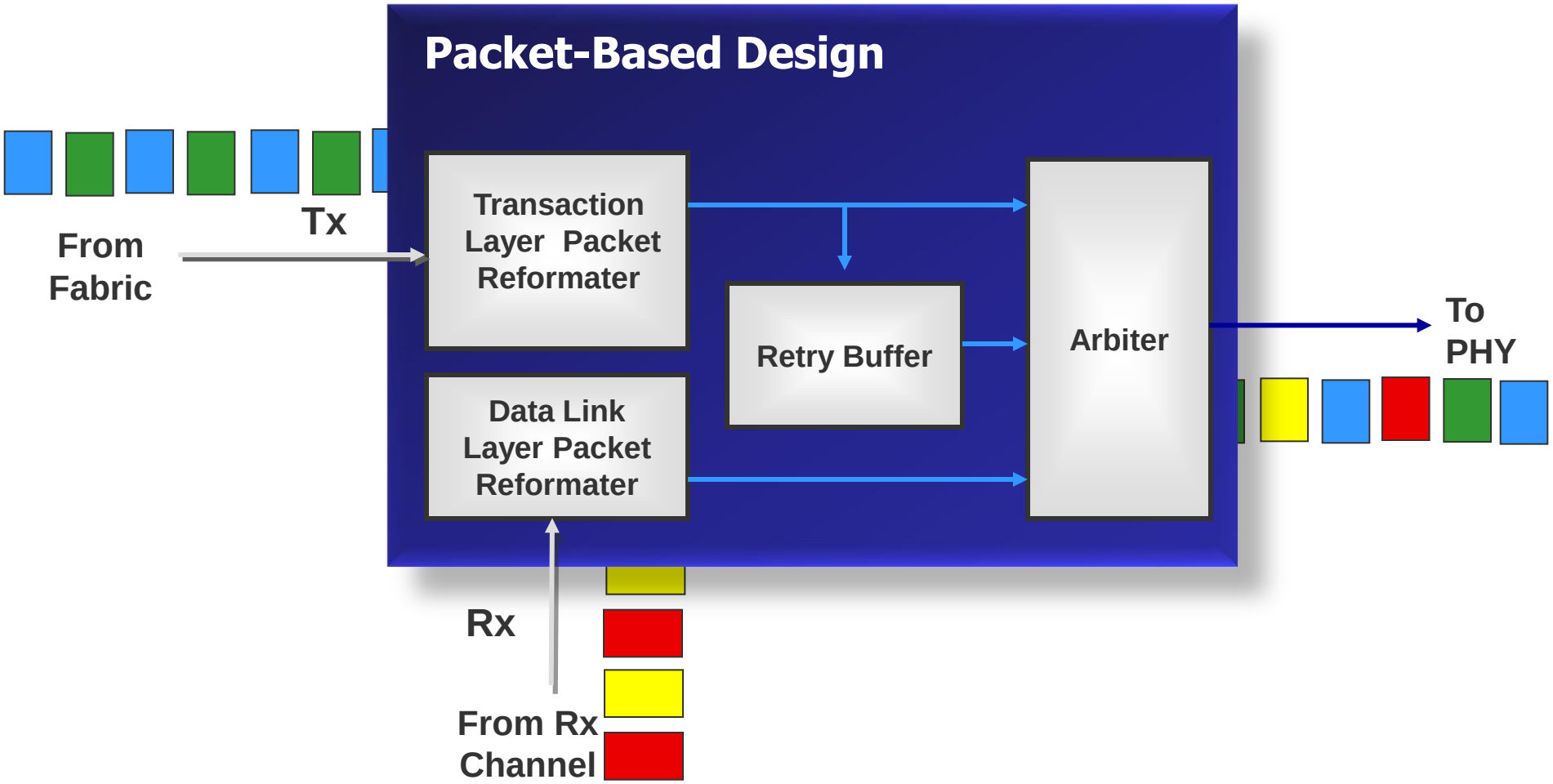

- Multiple, concurrent data streams
  - Cross bar
  - Bus traffic controller
  - DMA controller
  - Standard I/F (e.g., PCIe)
  - . . .

**Sequential data streams**
***1x* number of bugs**

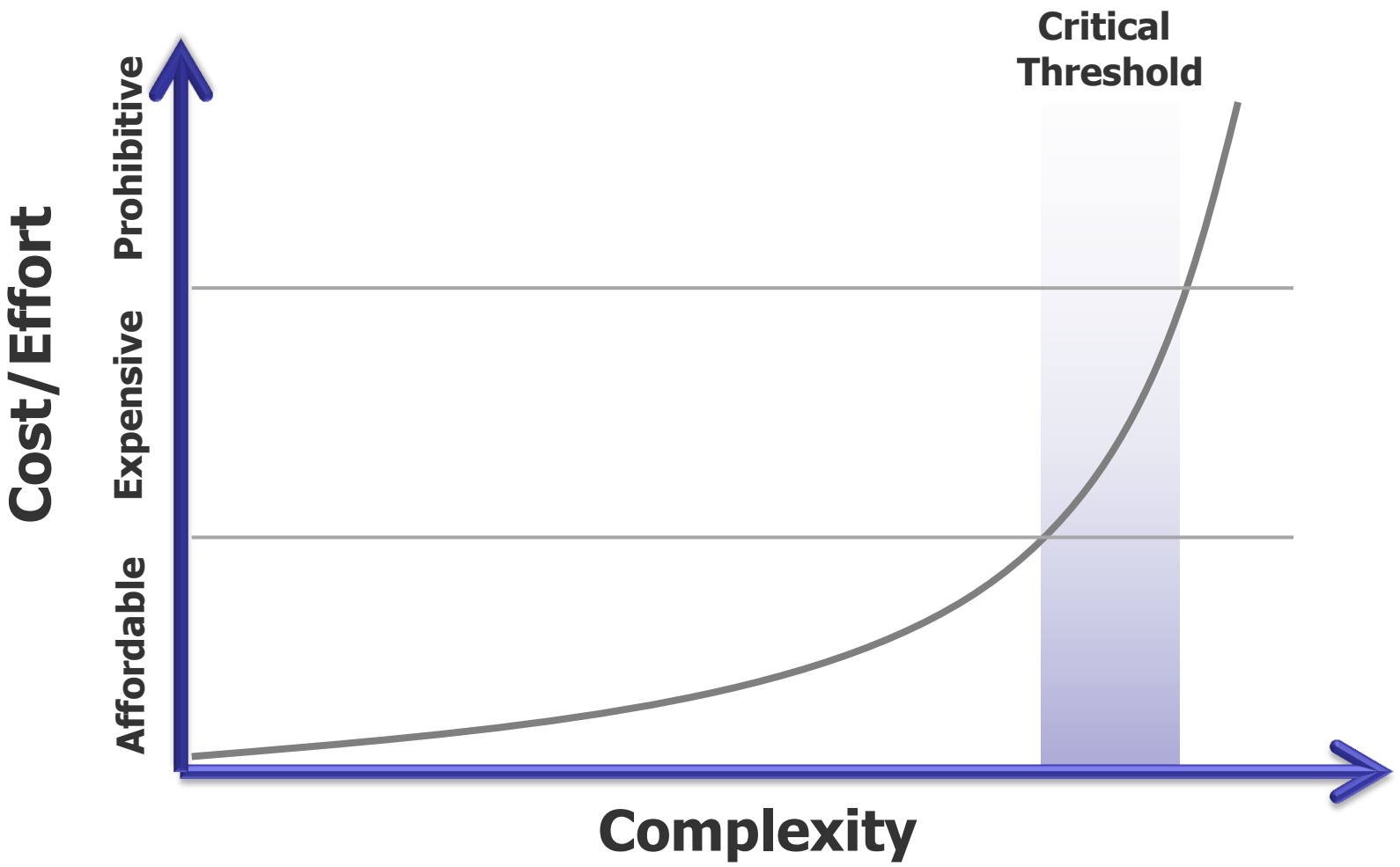
**Concurrent data streams**
***5x* number of bugs**

-Ted Scardamalia, internal IBM study

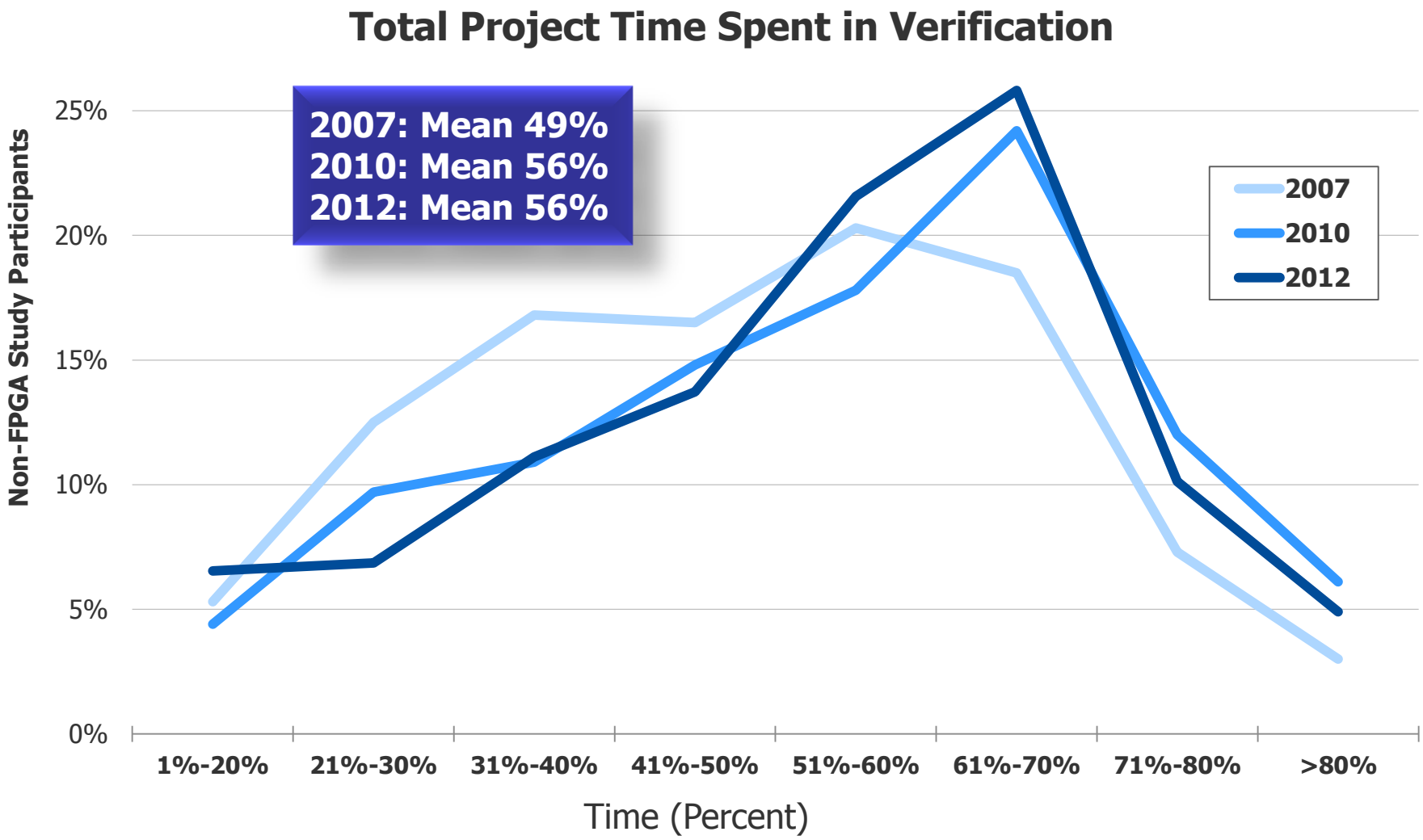
# Concurrency is Complicated to Verify



# Maybe effort is a good proxy?



# Verification Consumes Majority of Project Time

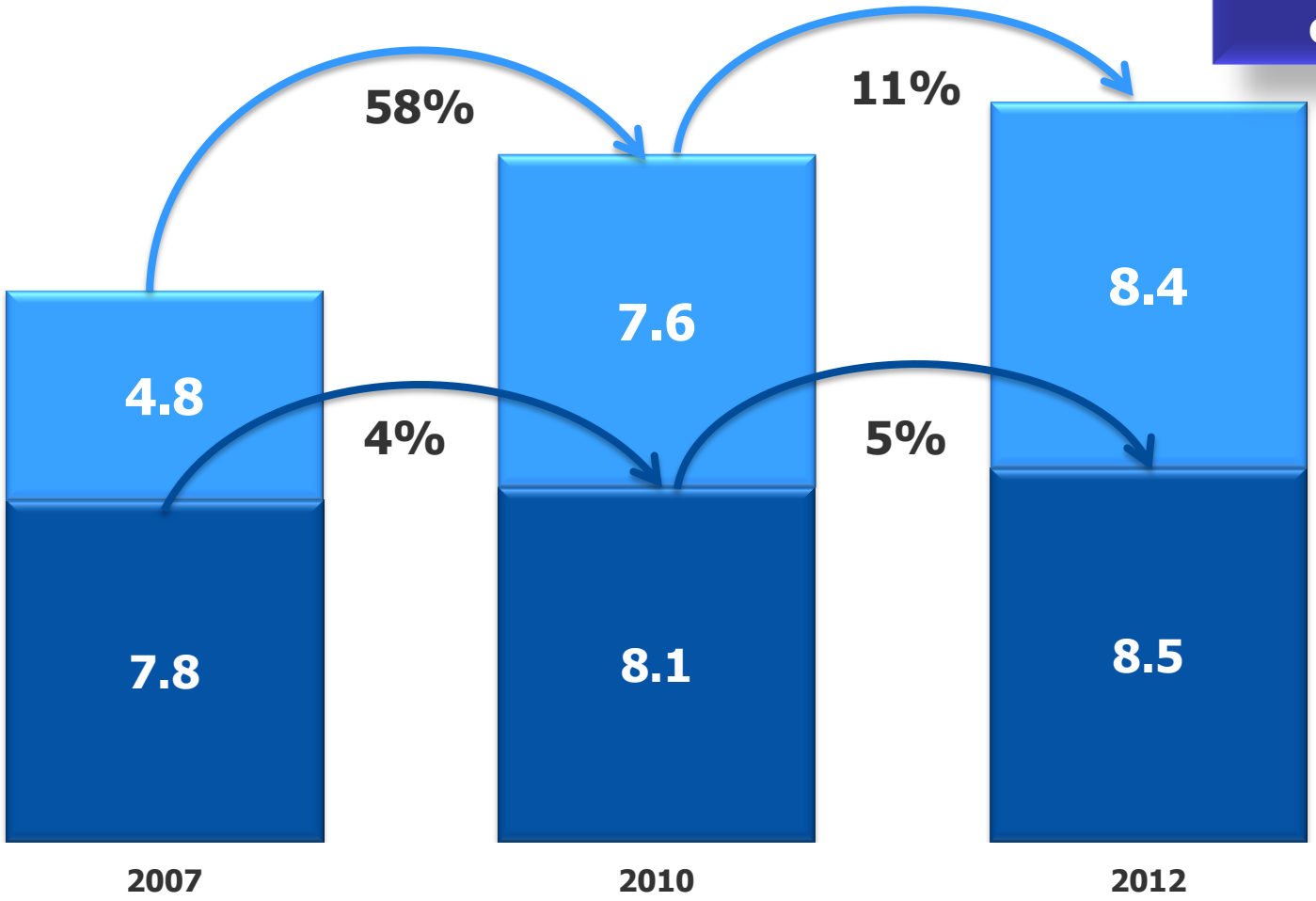



*Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# More and More Verification Engineers

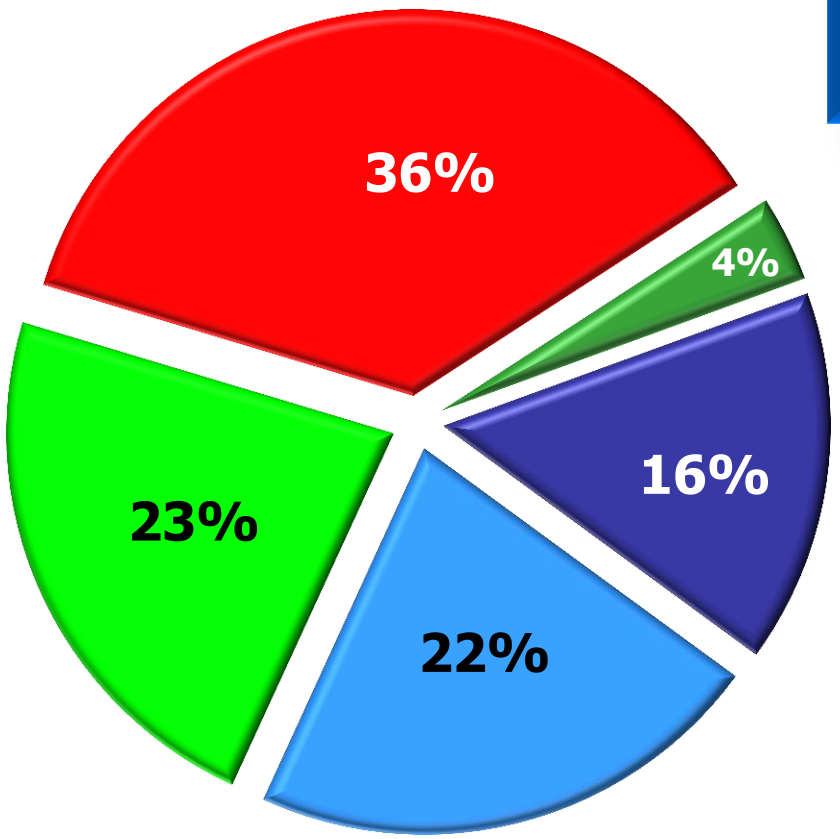
*Mean peak number of design vs. verification engineers*

**~ 1-to-1 ratio of peak design and verification engineers**




*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# Where Verification Engineers Spend Their Time

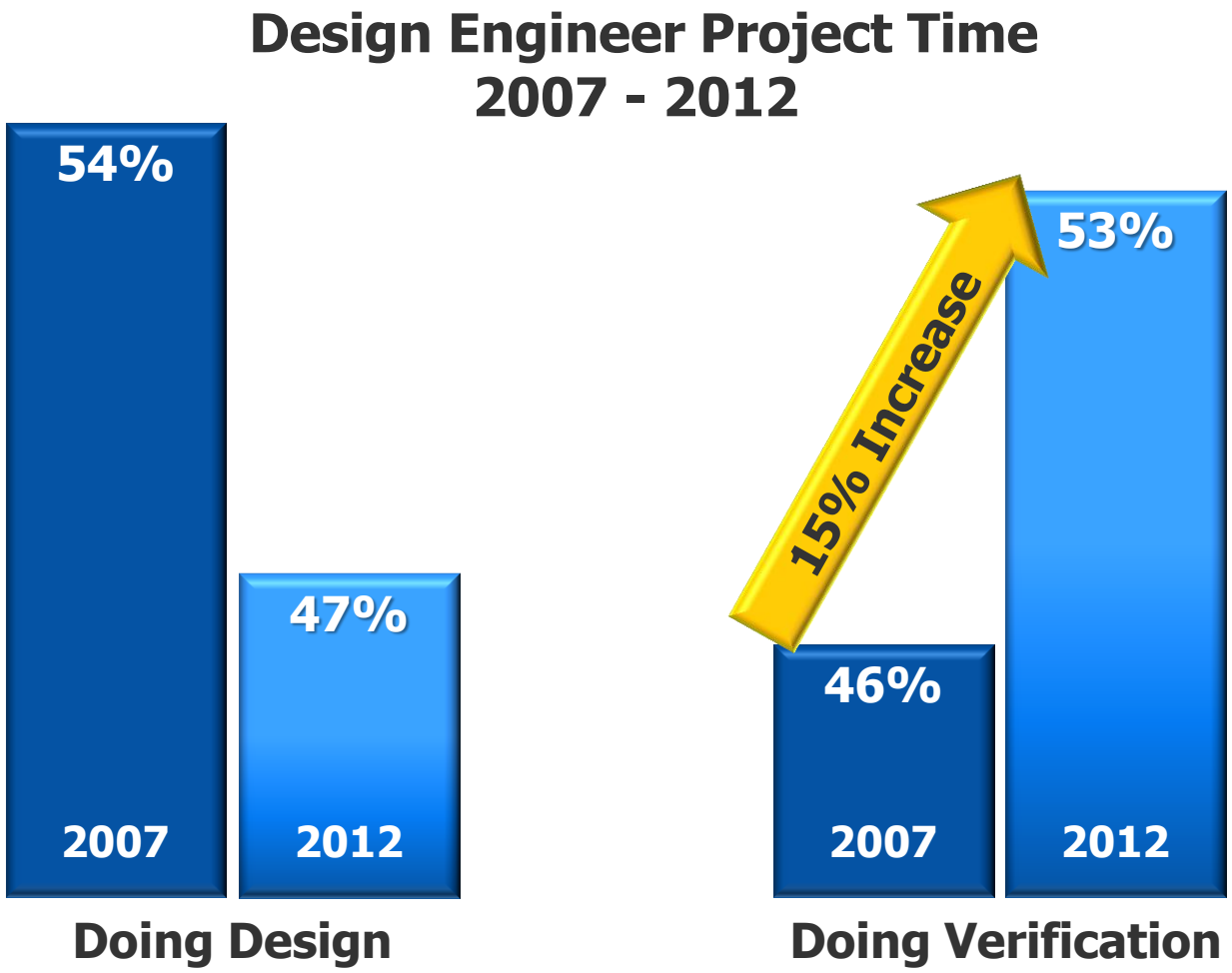



**More time spent in debug than any other task!**

- Test Planning
- Testbench Development
- Creating and Running Test
- Debug
- Other

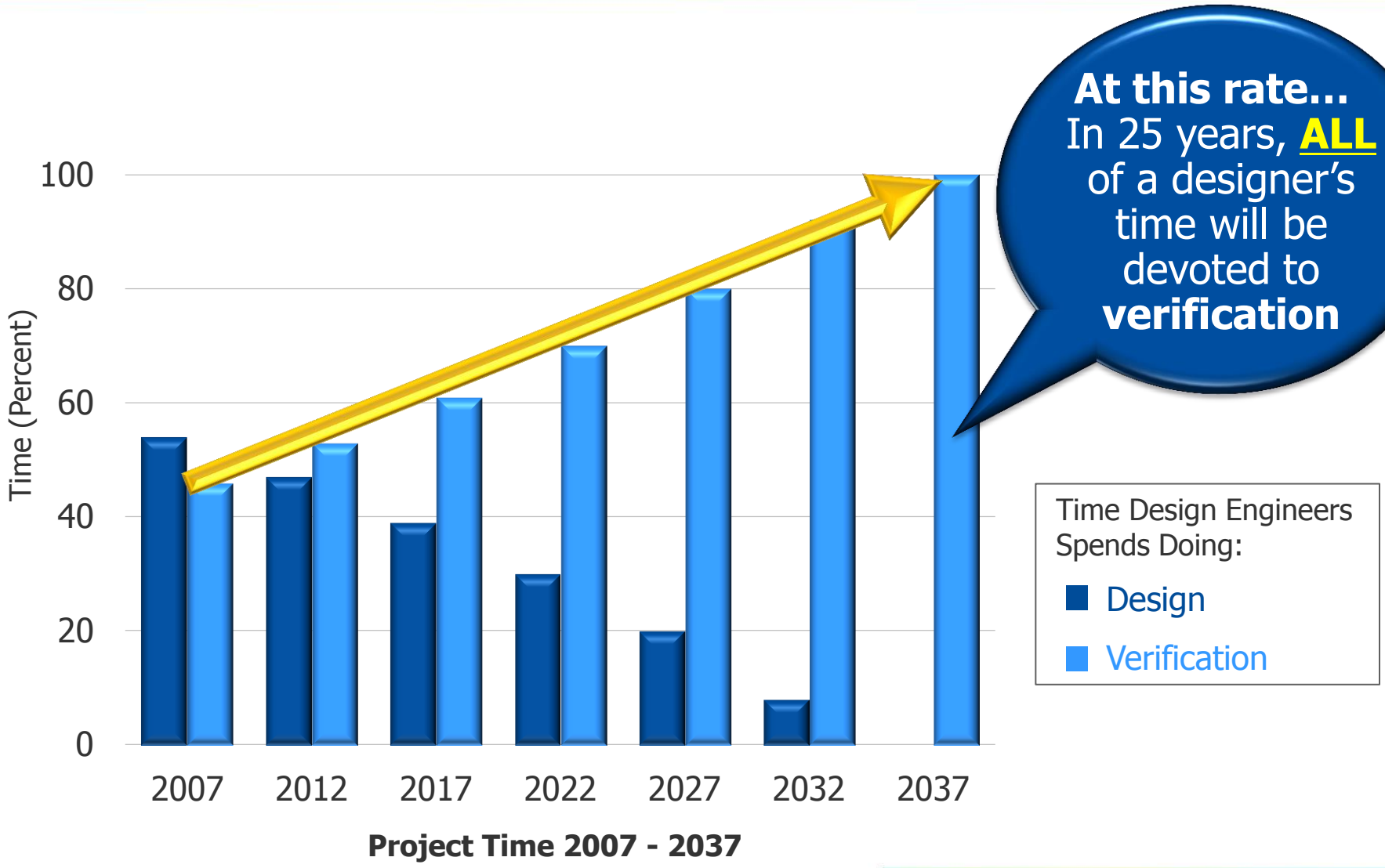
Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Designers Doing More and More Verification

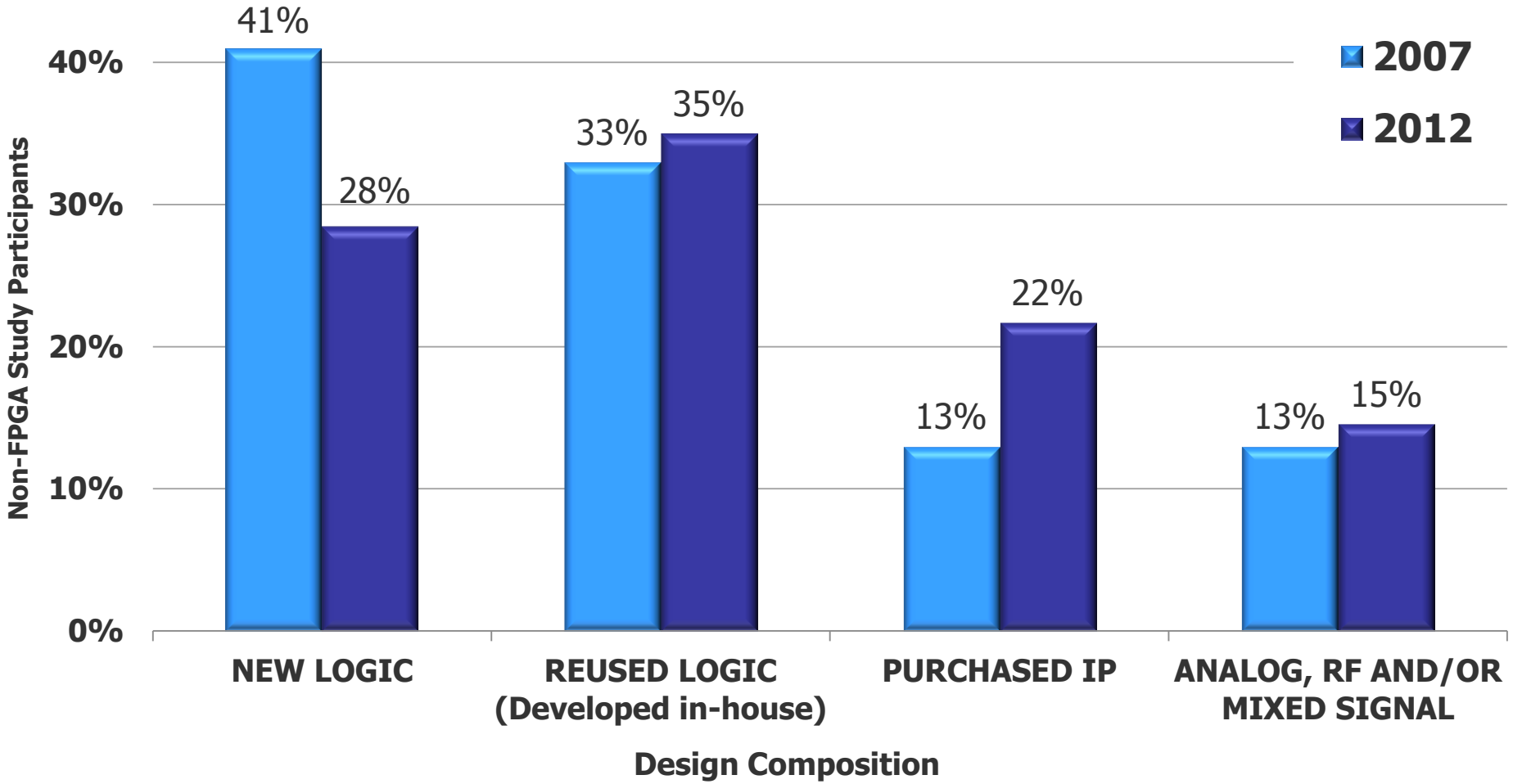



*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# Time Designers Spends in Design vs. Verification

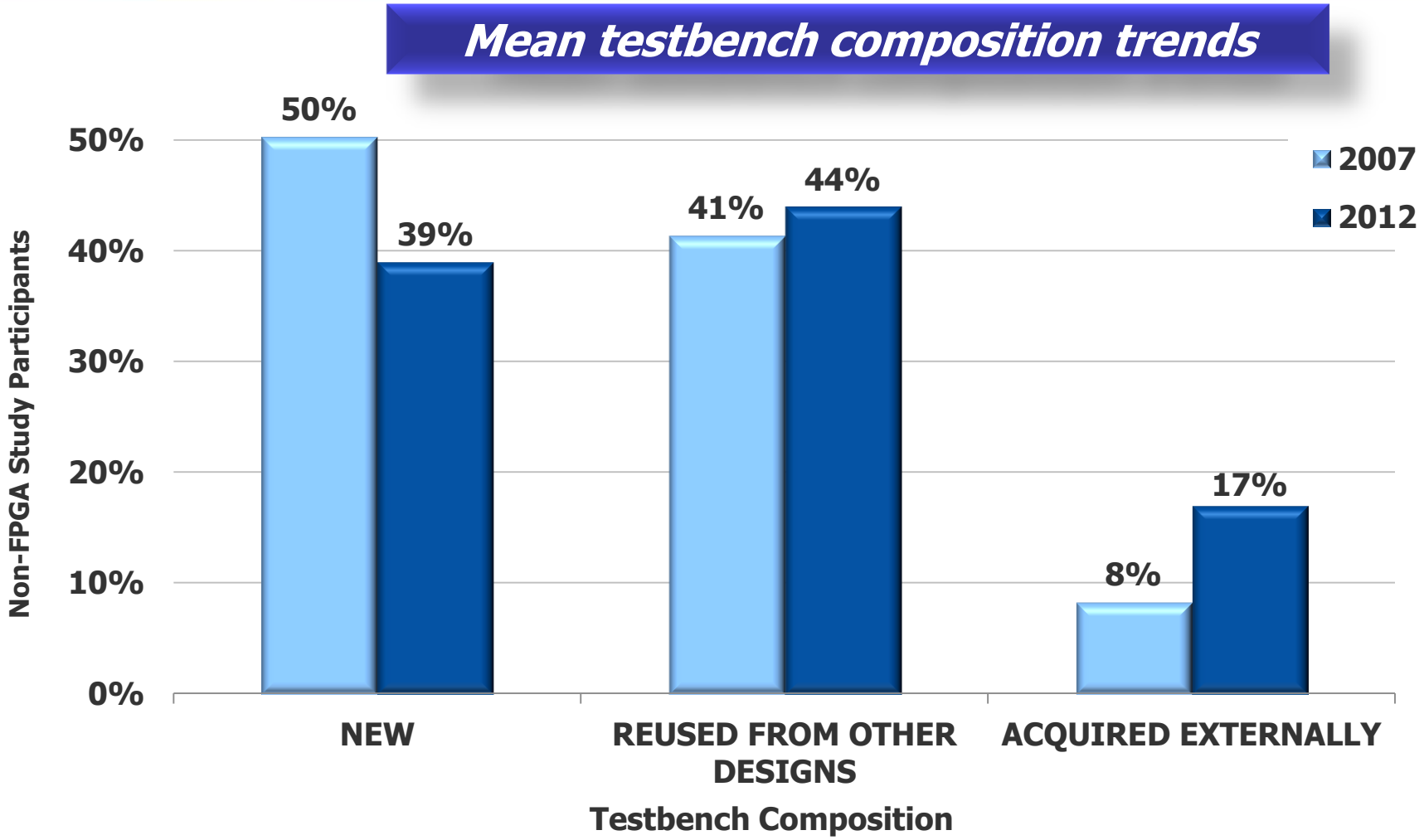


# Design Reuse Trends




Source: Wilson Research Group and Mentor Graphics.

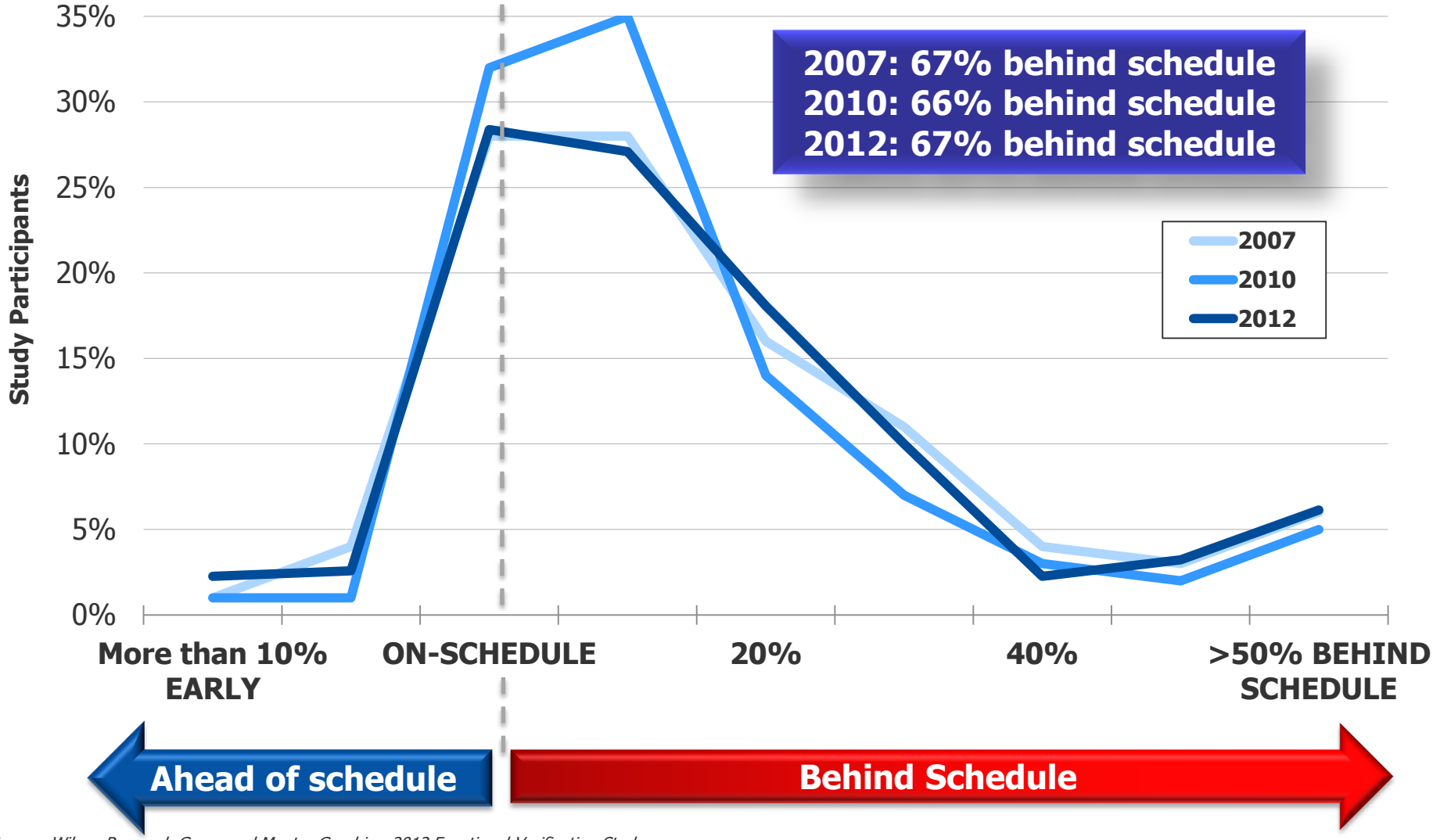
# Verification Reuse




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

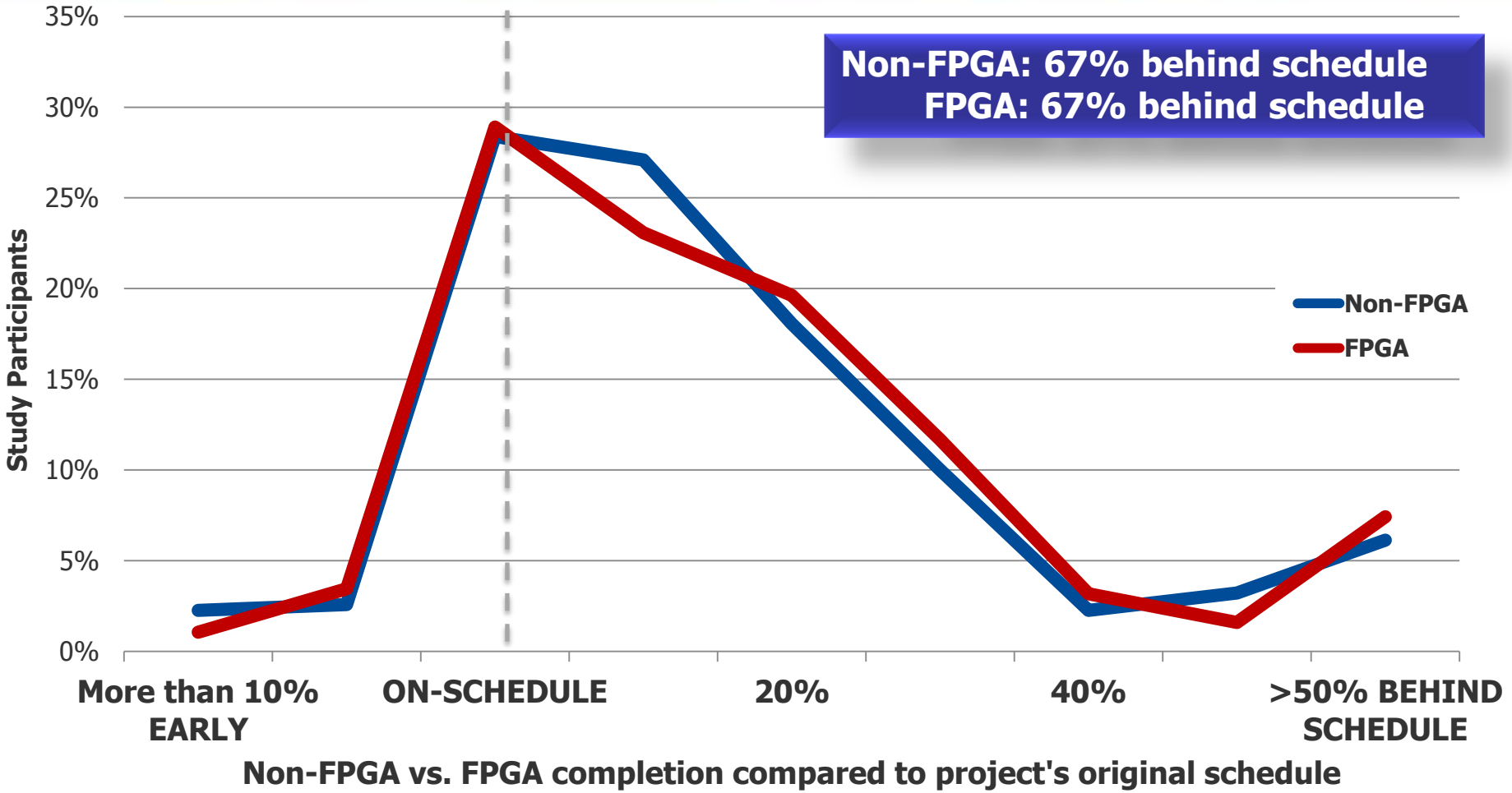
# With All This Effort, How are We Doing?

# Project's Schedule Completion Trends



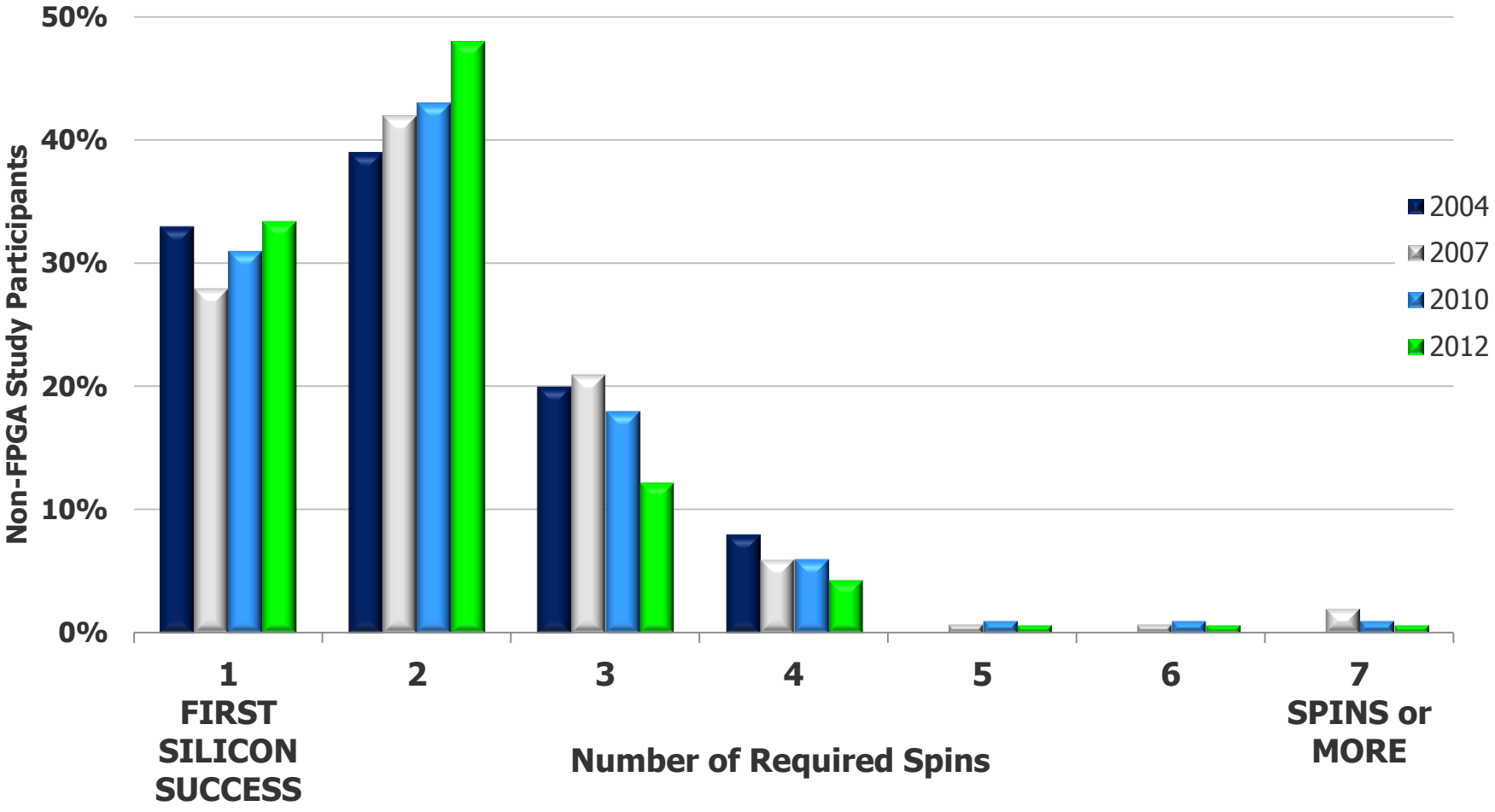

*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# FPGA vs. Non-FPGA Completion Trends



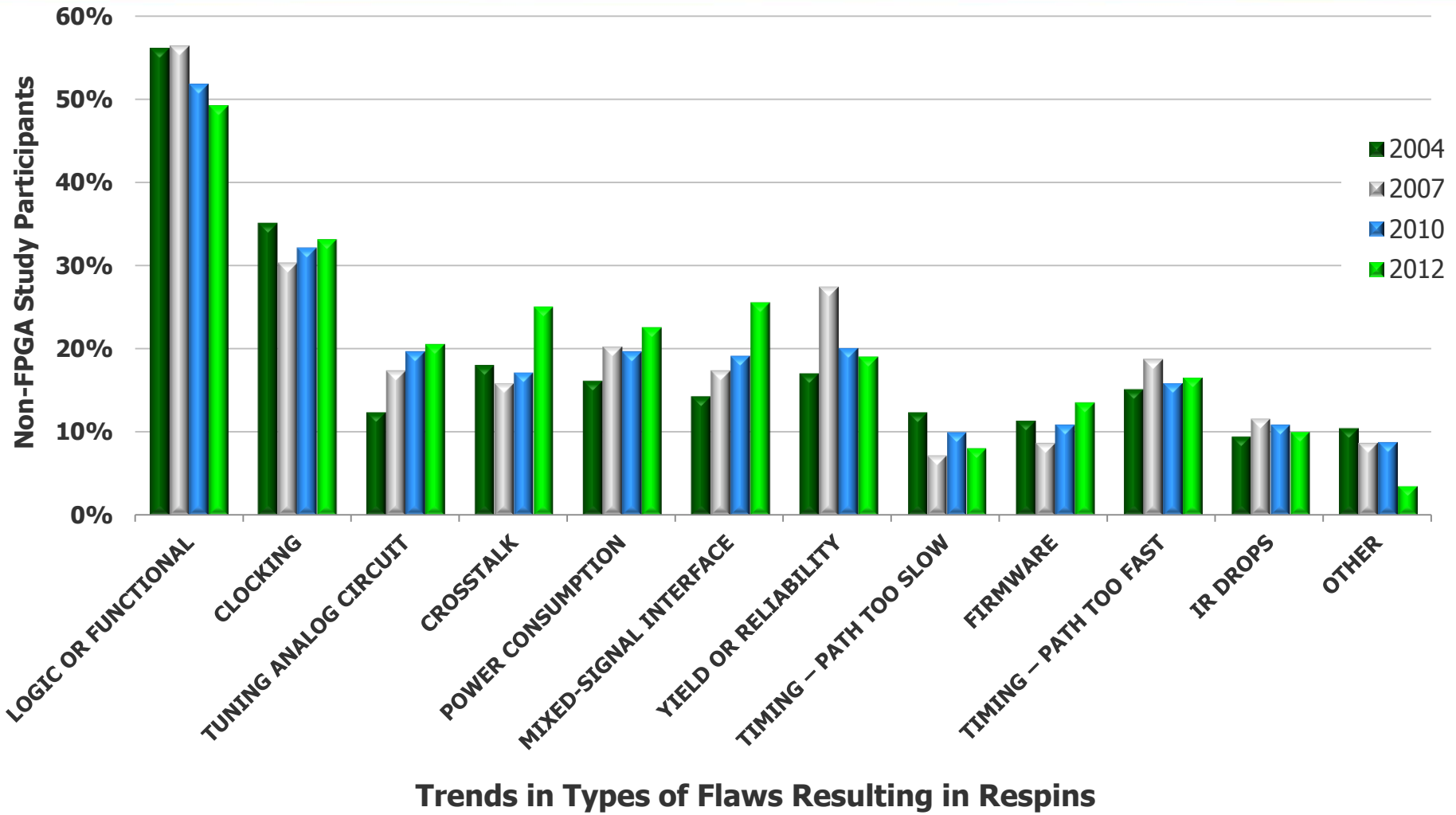

Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Required Number of Spins




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Types of Flaws

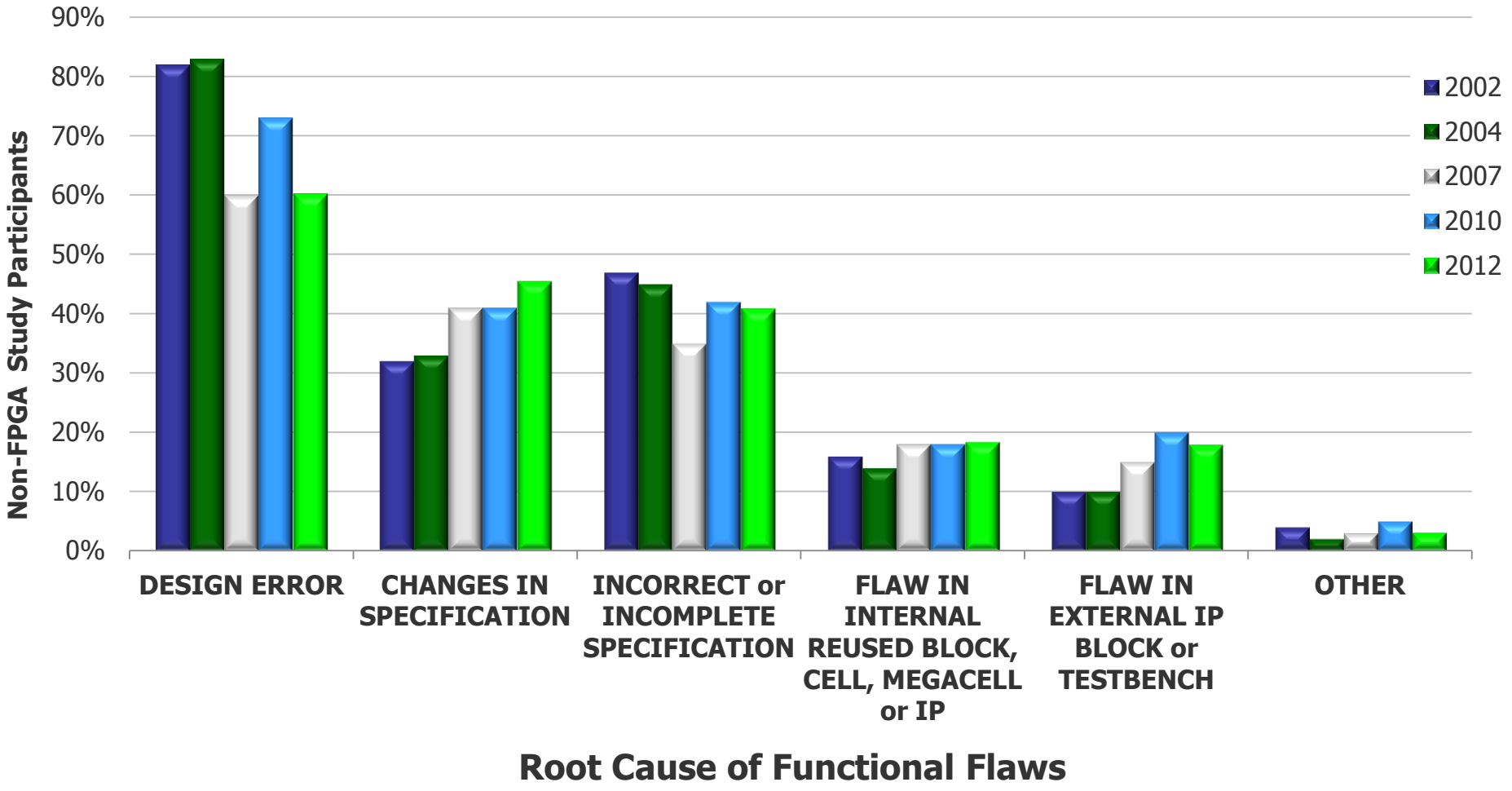



**Trends in Types of Flaws Resulting in Respins**

Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

* Multiple answers possible

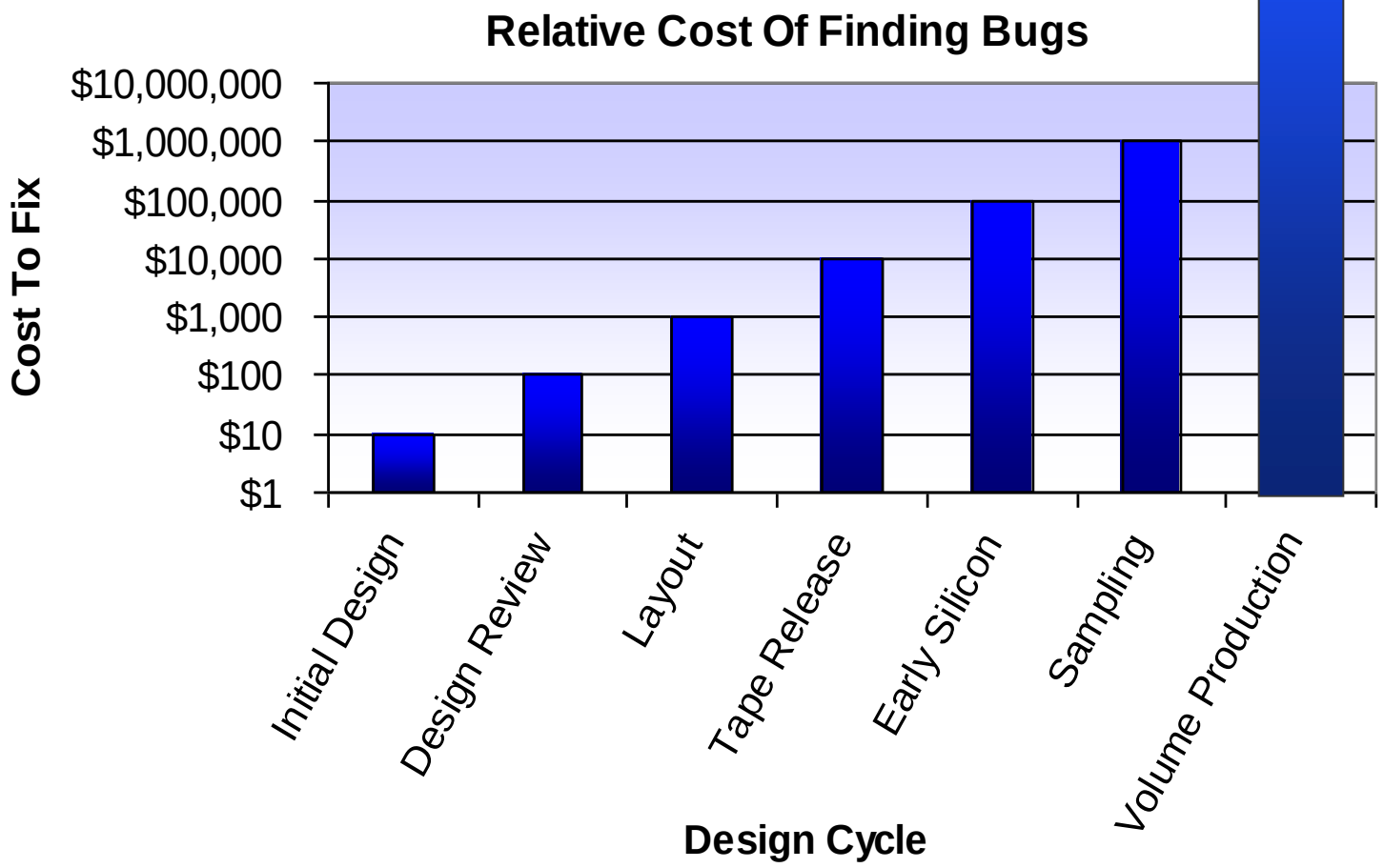
# Root Cause of Functional Flaws




Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

* Multiple answers possible

# Cost of Find Functional Flaws

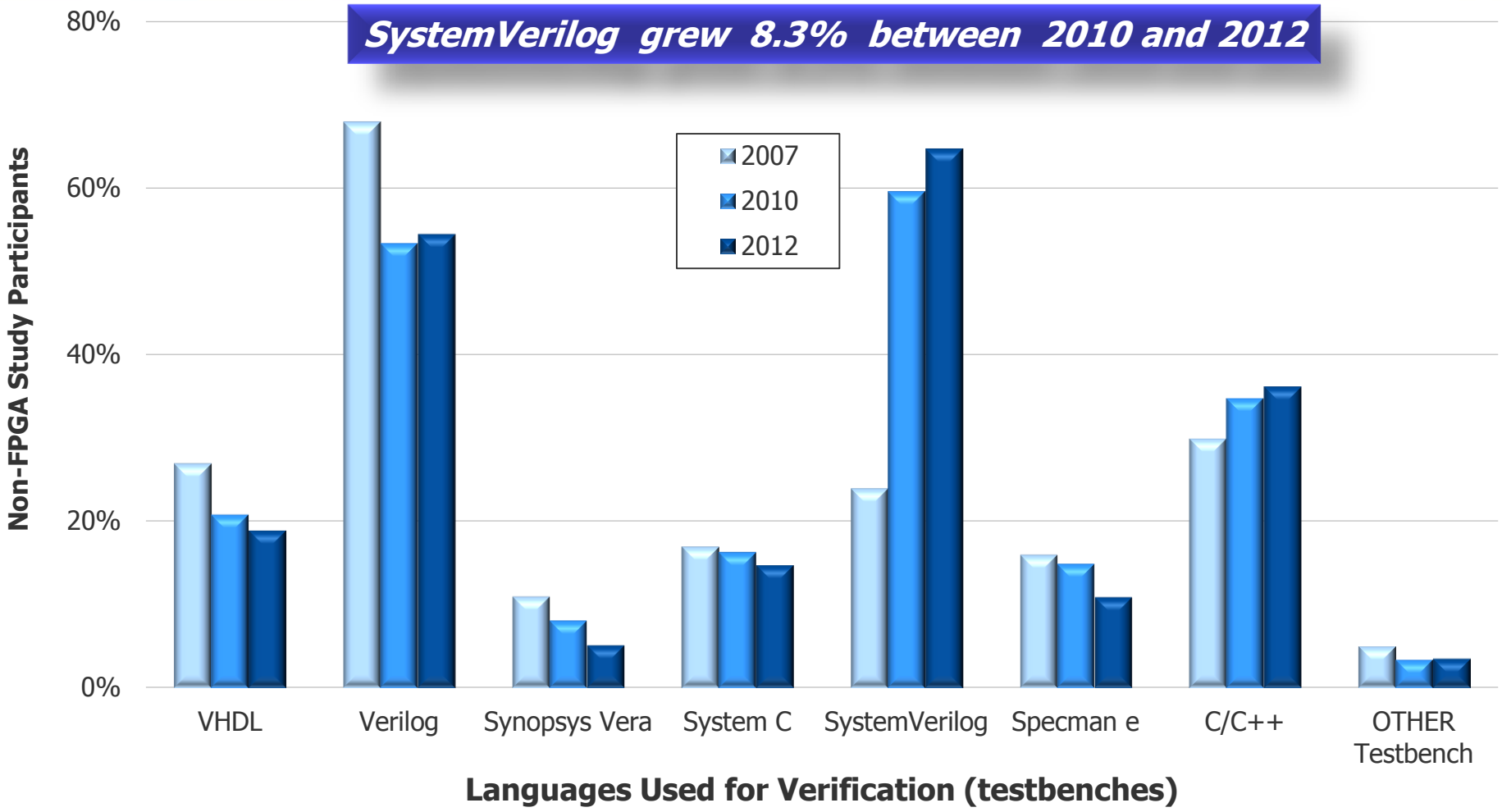



Silicon Debug, Doug Josephson and Bob Gottlieb, (Paul Ryan)
*D. Gizopoulos (ed.), Advances in Electronic Testing: Challenges and Methodologies, Springer, 2006*

Beyond arguing over who won the standards war

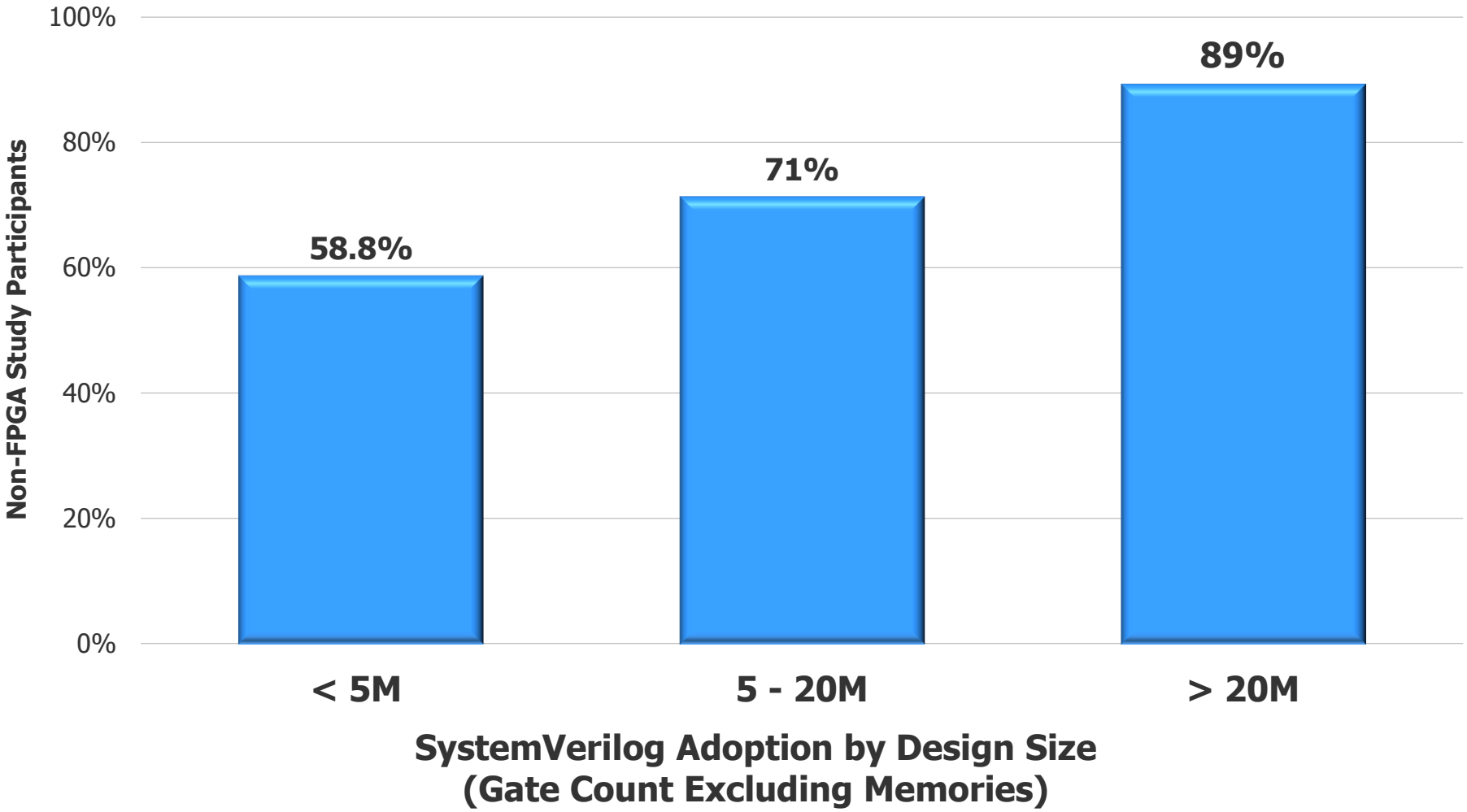
# BEYOND STANDARDS

# Standardization of Languages



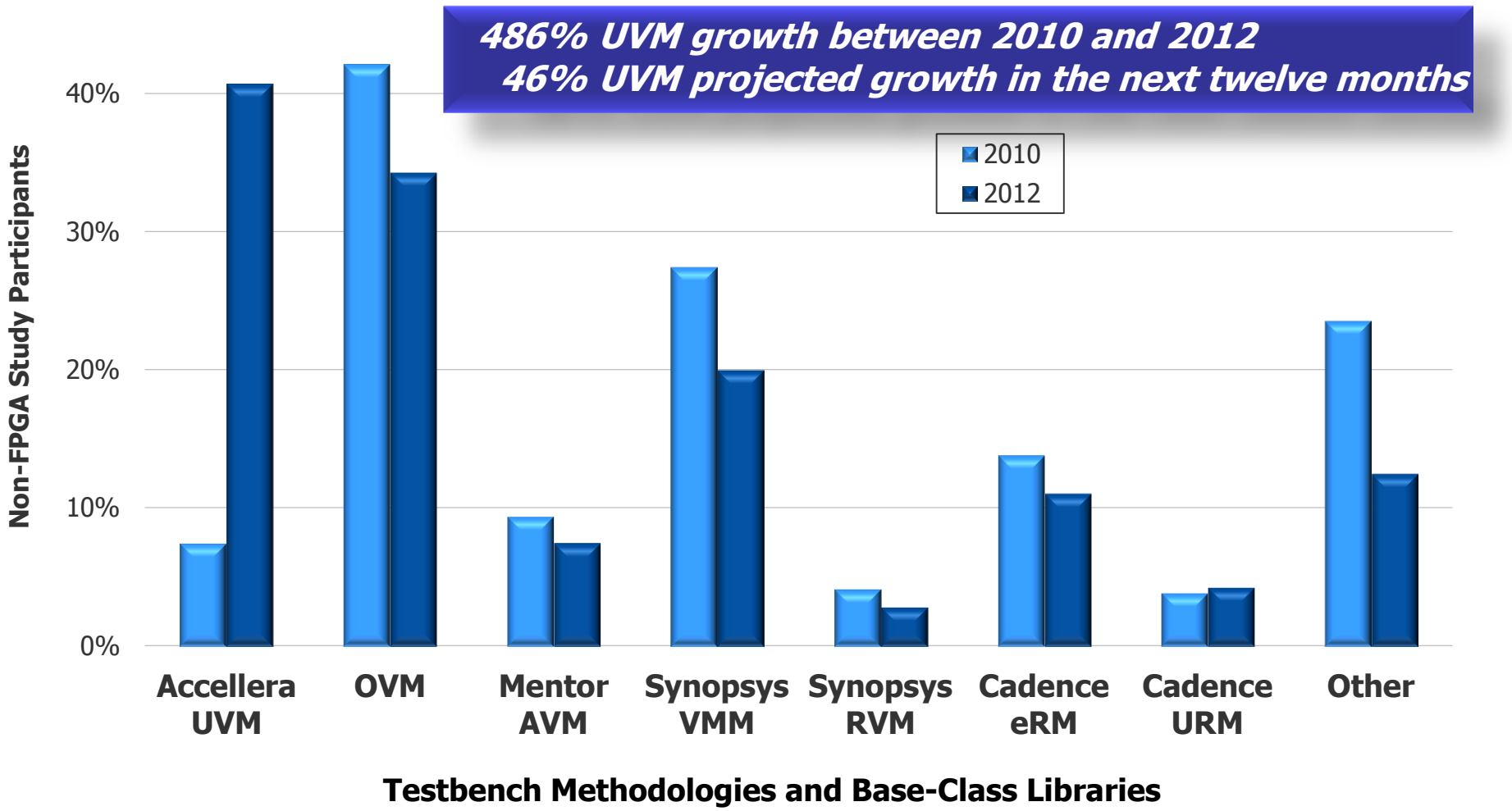

*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

# SystemVerilog Adoption by Design Size




*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

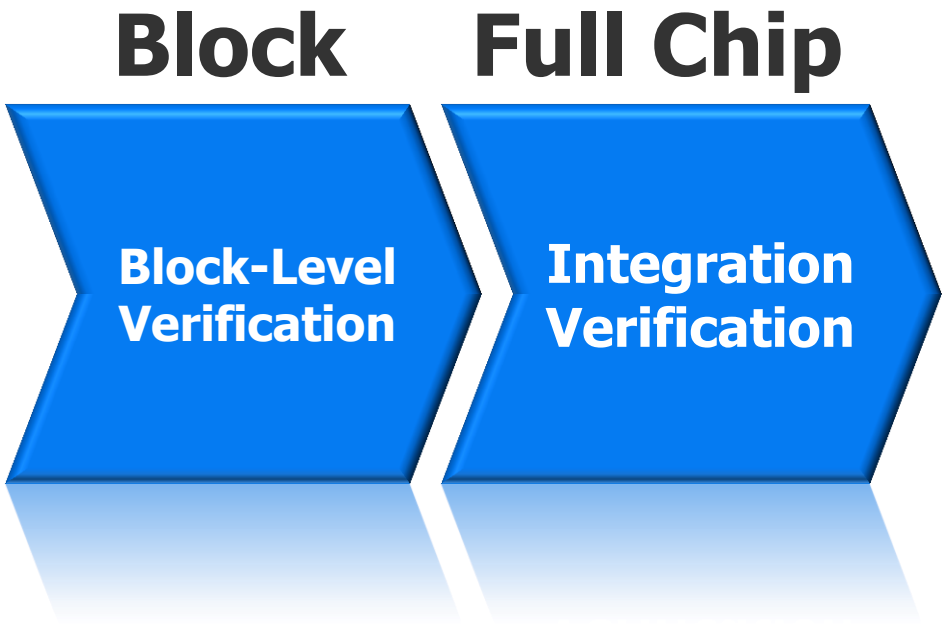
# Standardization in Base Class Libraries




*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study*

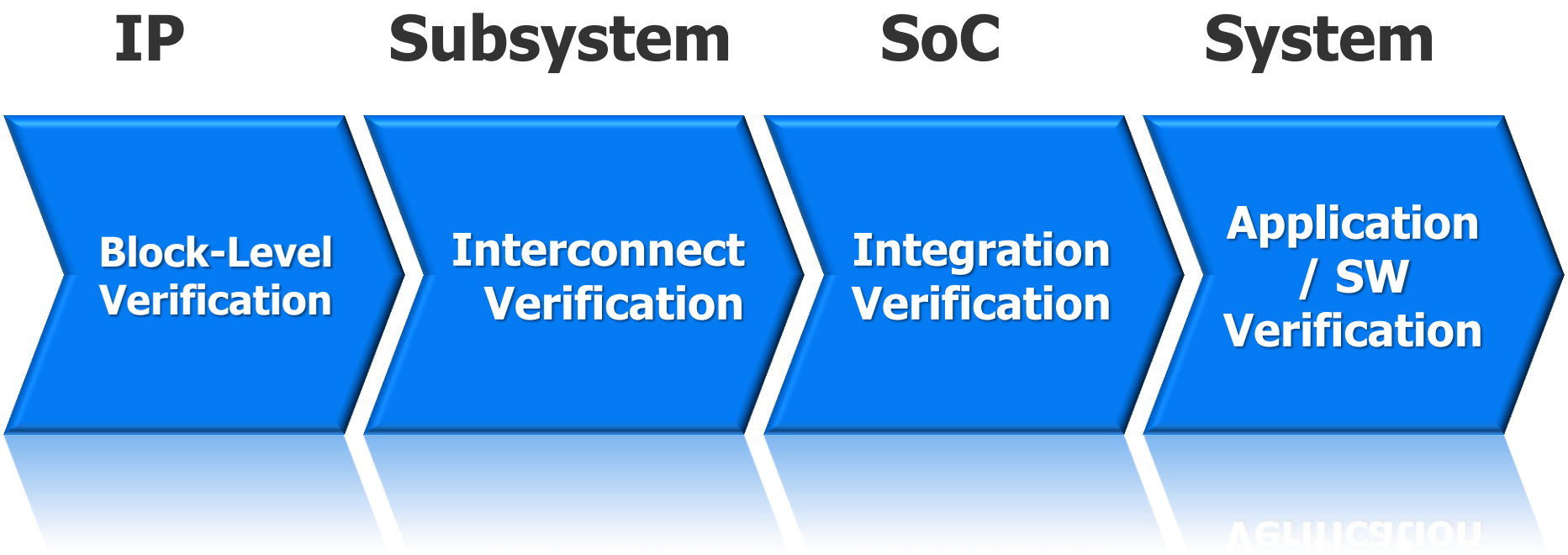
# Standardization of the SoC Verification Process

- Ten years ago, IC/ASIC verification was partitioned into two main steps:



# Standardization of the SoC Verification Process

- Emerging from *ad hoc* to systematic processes

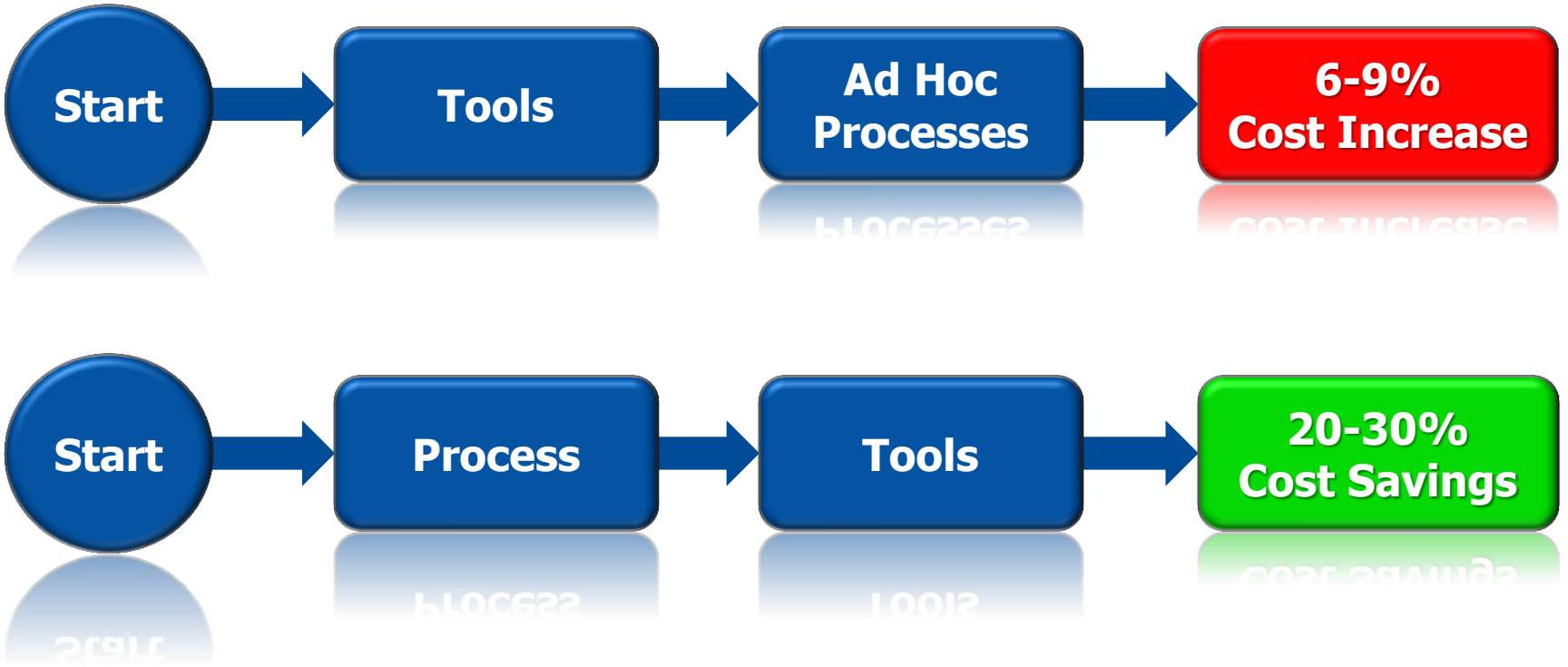


Beyond surviving by maintaining the status quo

# BEYOND THE STATUS QUO

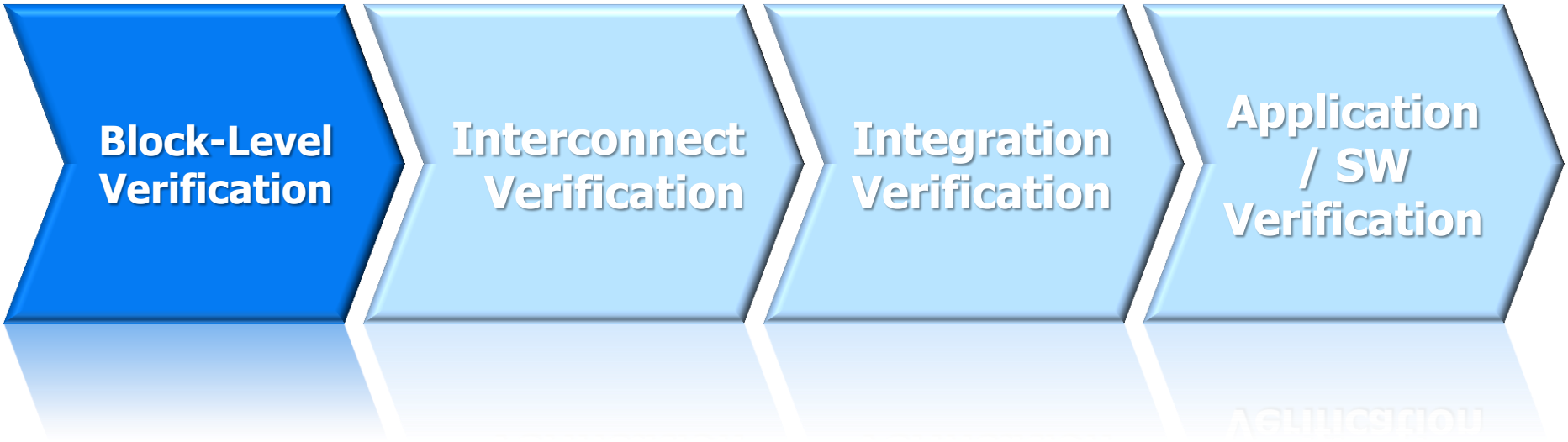
# The Verification Paradox

- A good verification process lets you get the most out of best-in-class verification tools

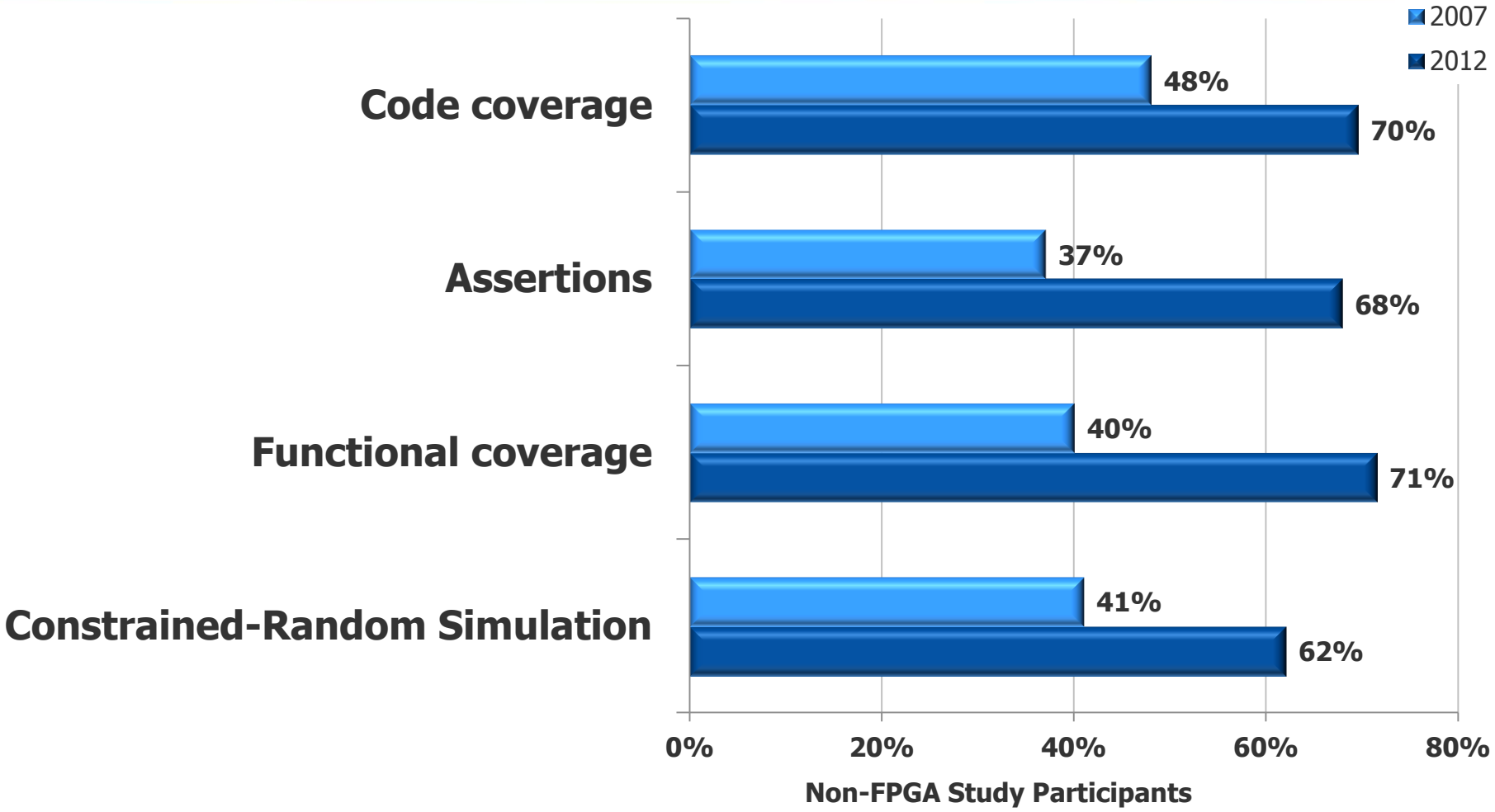



*Source: Cisco Momentum Research Group*

# Standardization of the SoC Verification Process

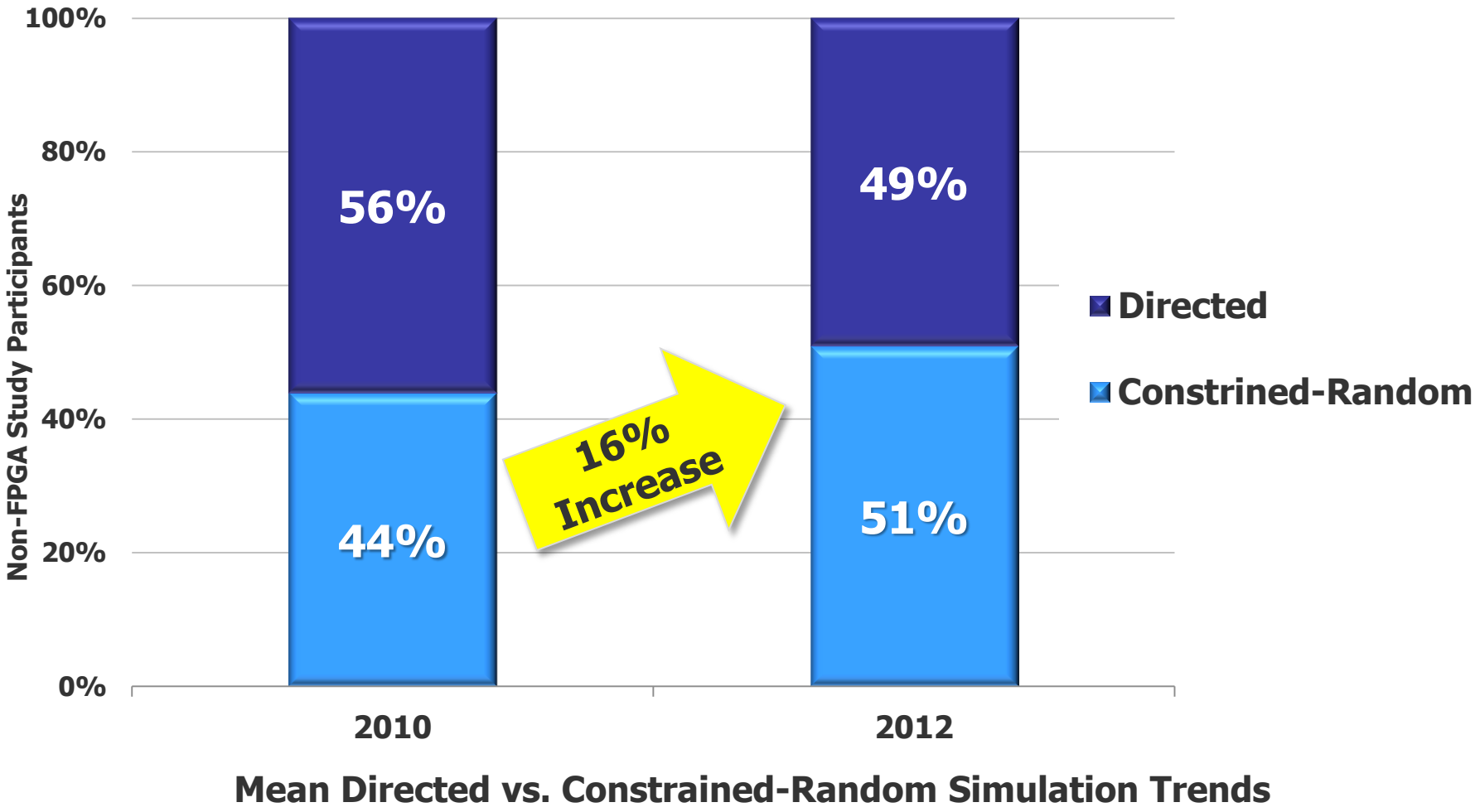


# Use of Advanced Verification Techniques




Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study

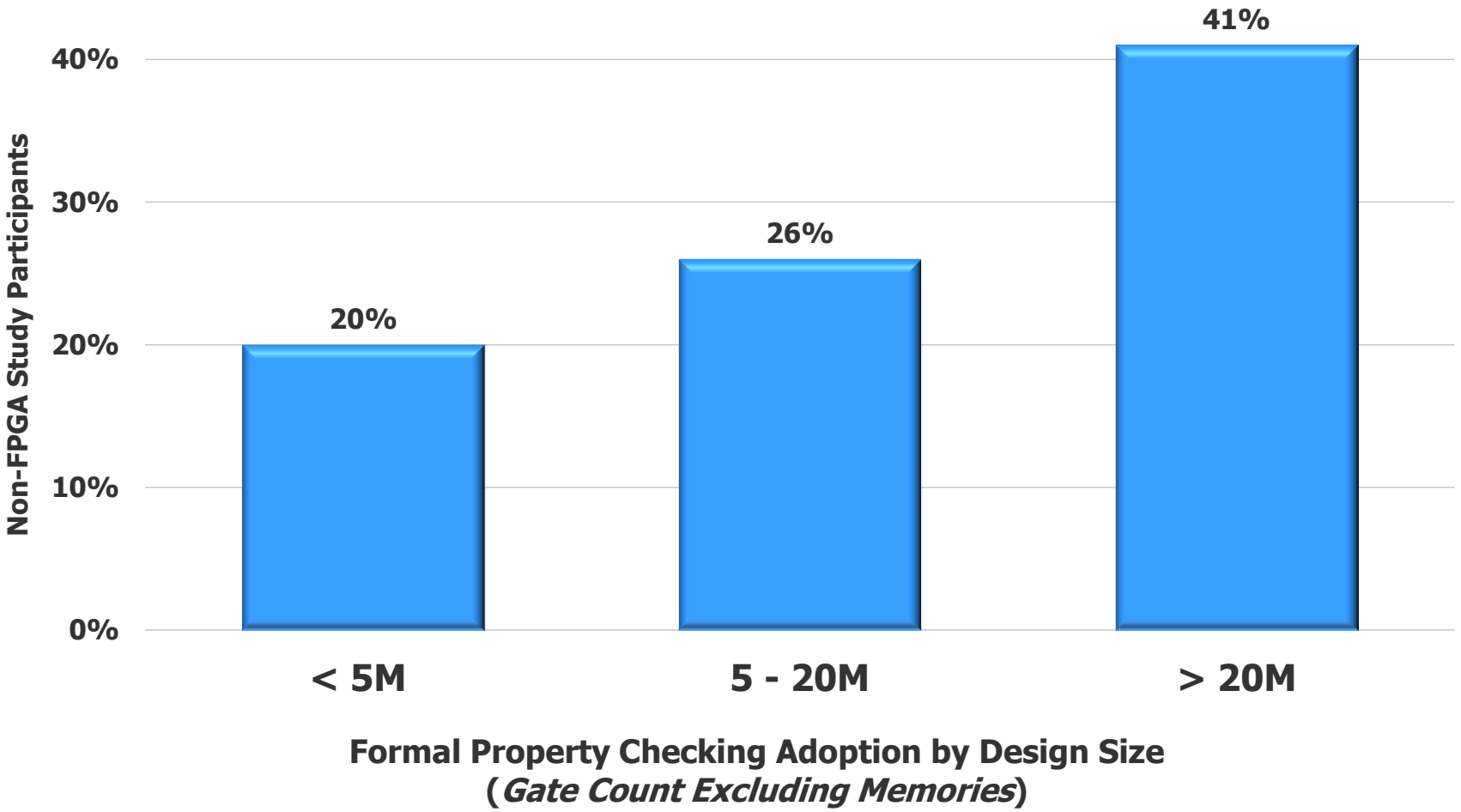
# Directed vs Constrained-Random Simulation




**Mean Directed vs. Constrained-Random Simulation Trends**

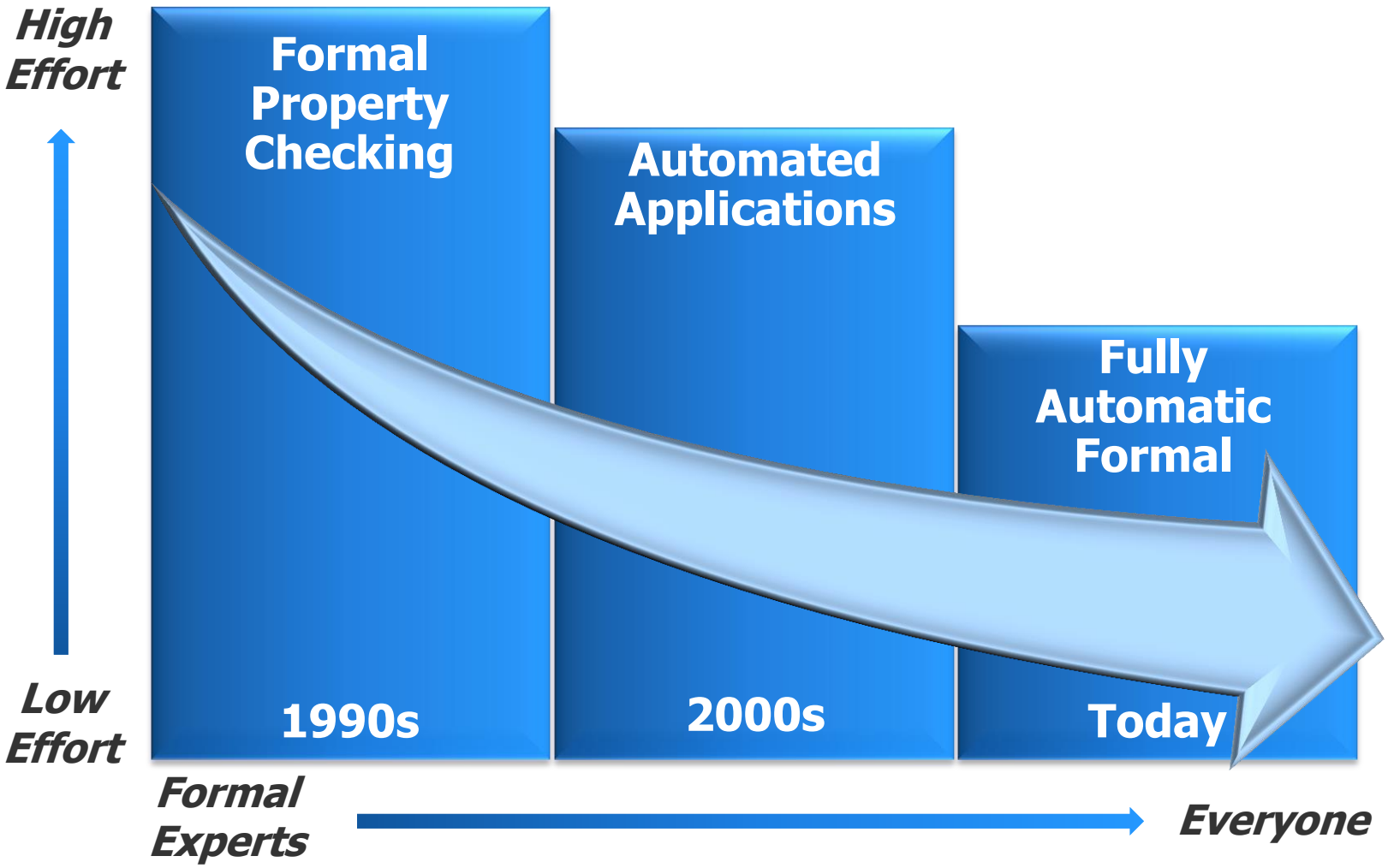
Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

# Larger Designs Use More Formal




Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study

# The Evolution of Formal Technology



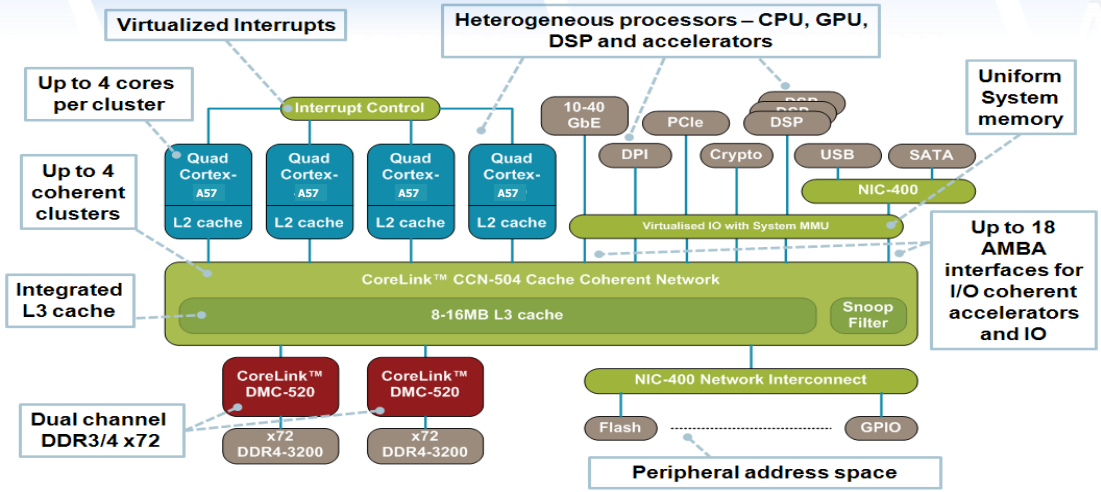
# Standardization of the SoC Verification Process

Block-Level Verification

**Interconnect Verification**

Integration Verification

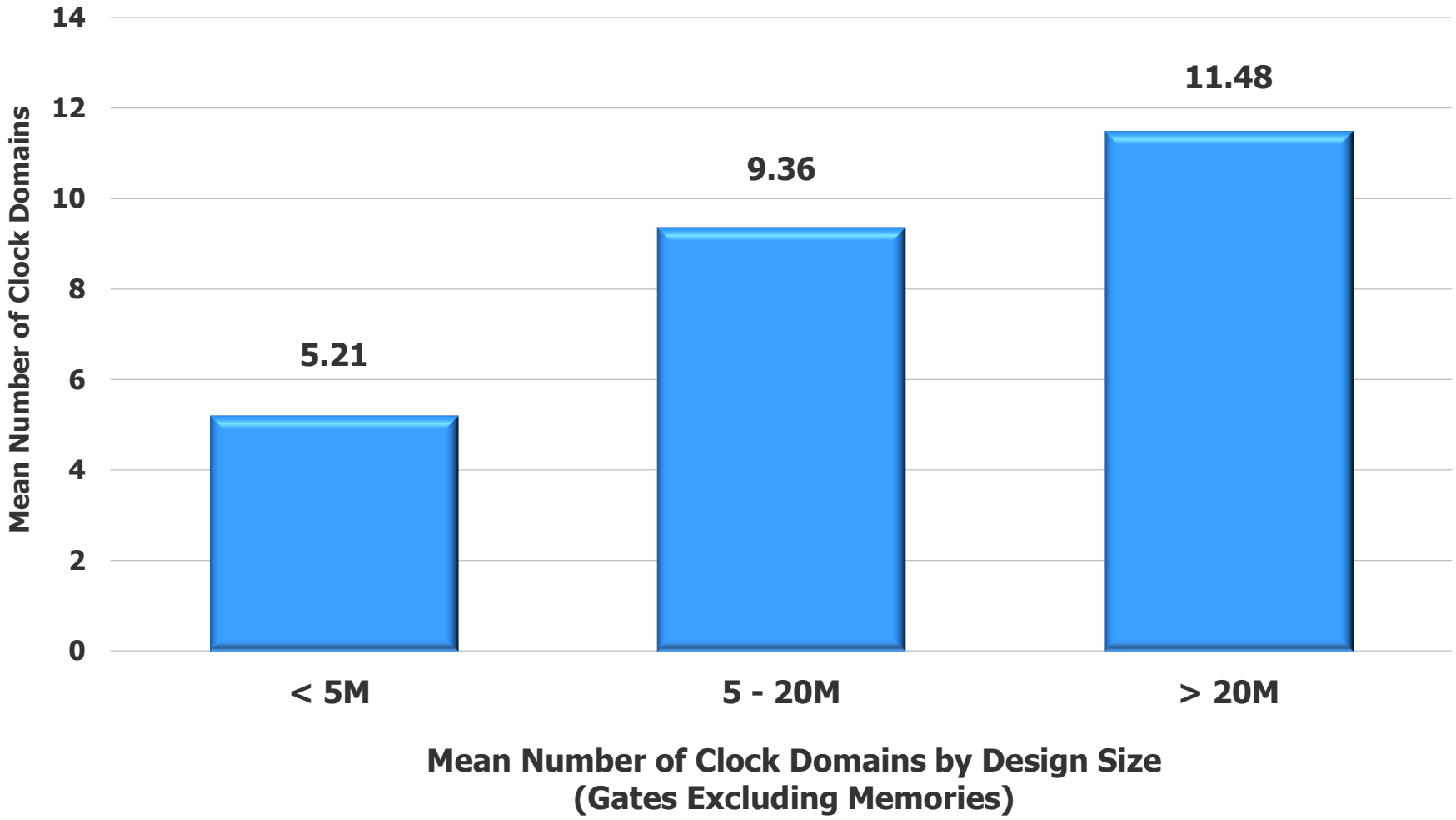
Application / SW Verification



# Standardization of the SoC Verification Process


- IP Blocks connectivity
- Access all memories
- Access all registers, such as control
- Configurations work
- Functional scenarios and use-cases
- Verify multiple clock domain crossings

# Mean Number of Clock Domains by Design Size



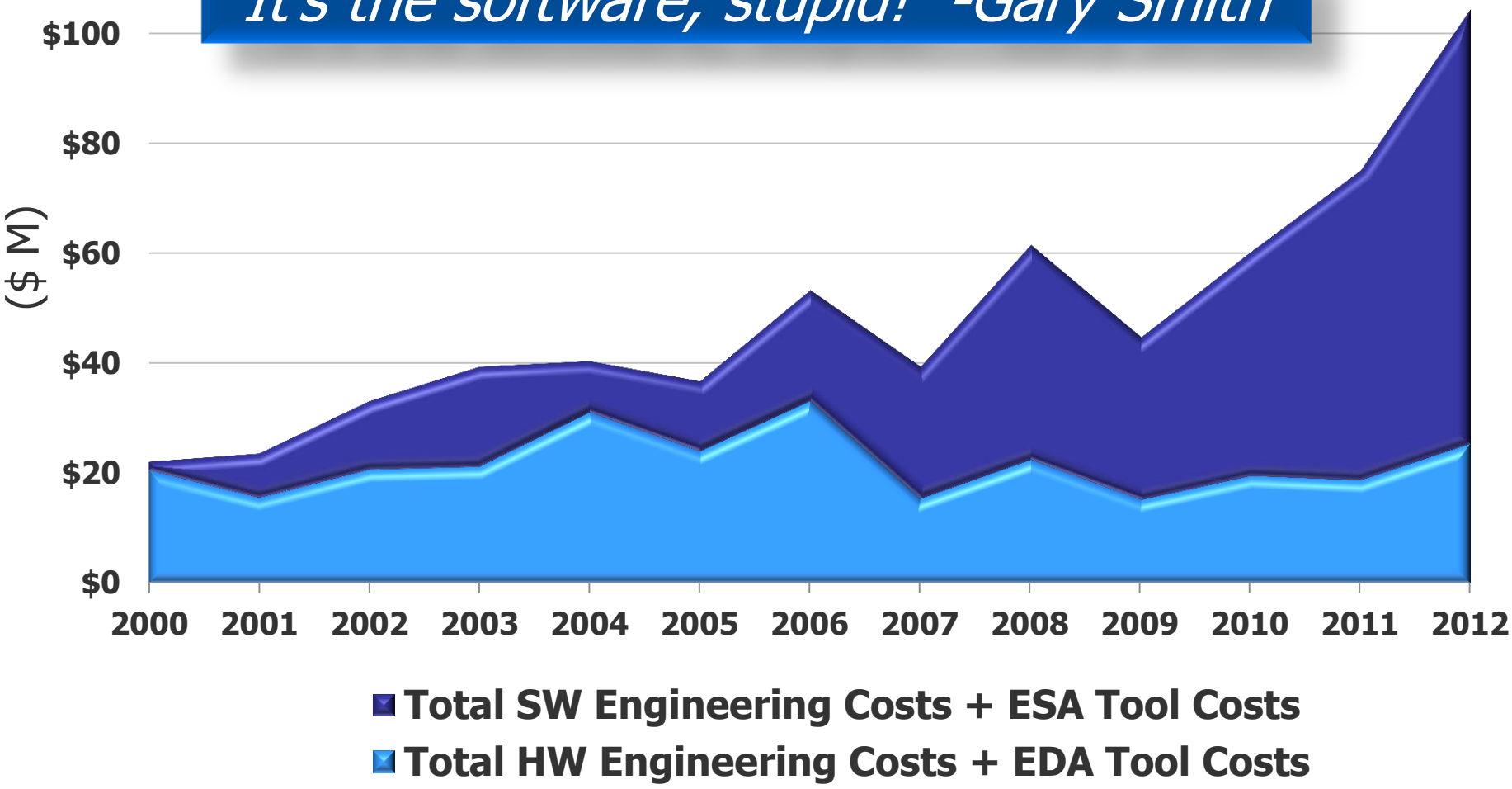

Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study

# Standardization of the SoC Verification Process


- Boot OS
- Load System Drivers
- Run Application SW

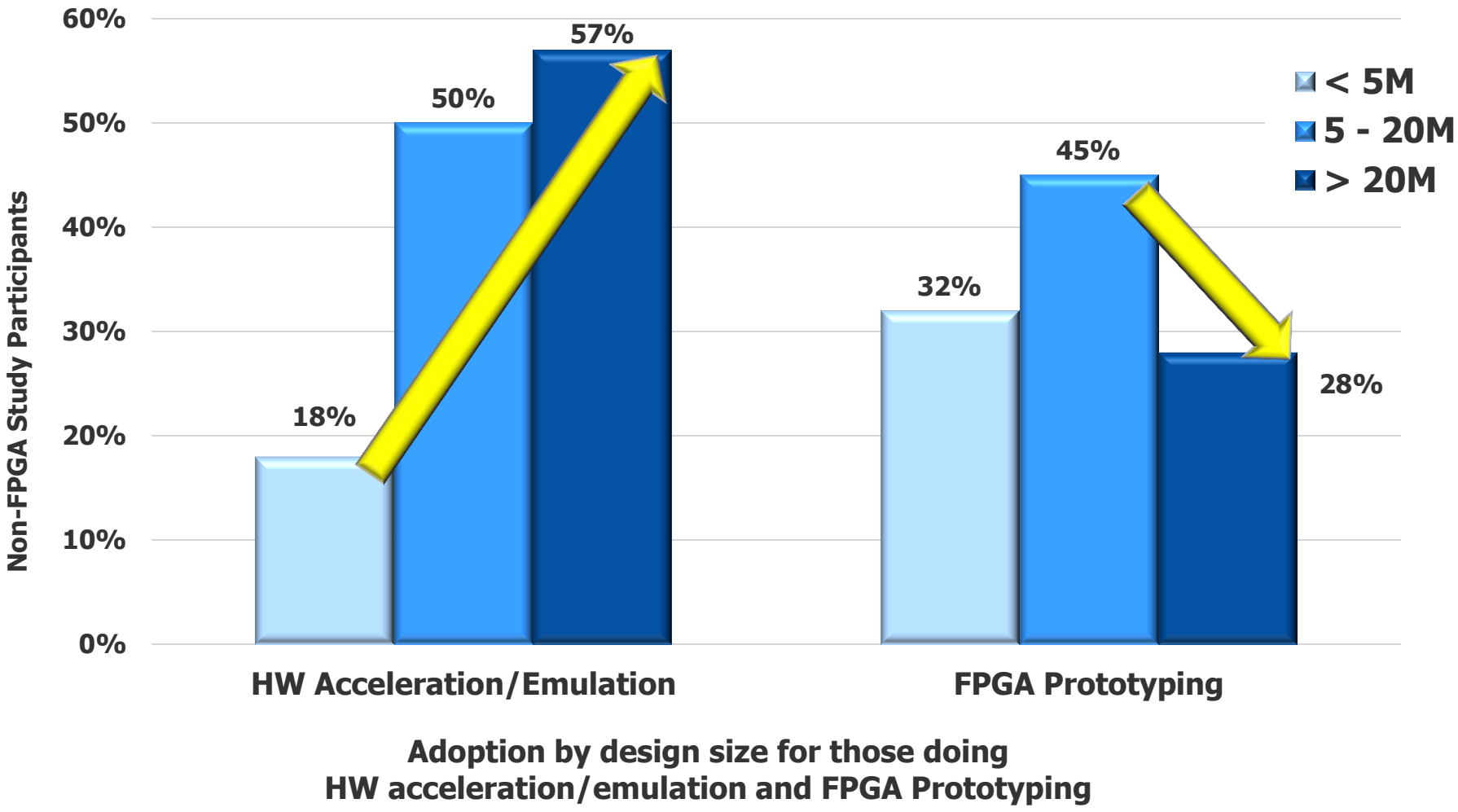
# SoC Design & Verification Involves Lots of SW

*It's the software, stupid! -Gary Smith*




***Source: ITRS 2010, Impact of Design Technology on SoC Consumer Portable Implementation Cost***

# As Design Sizes Increase…Emulation Up, FPGA Prototyping Down in 2012



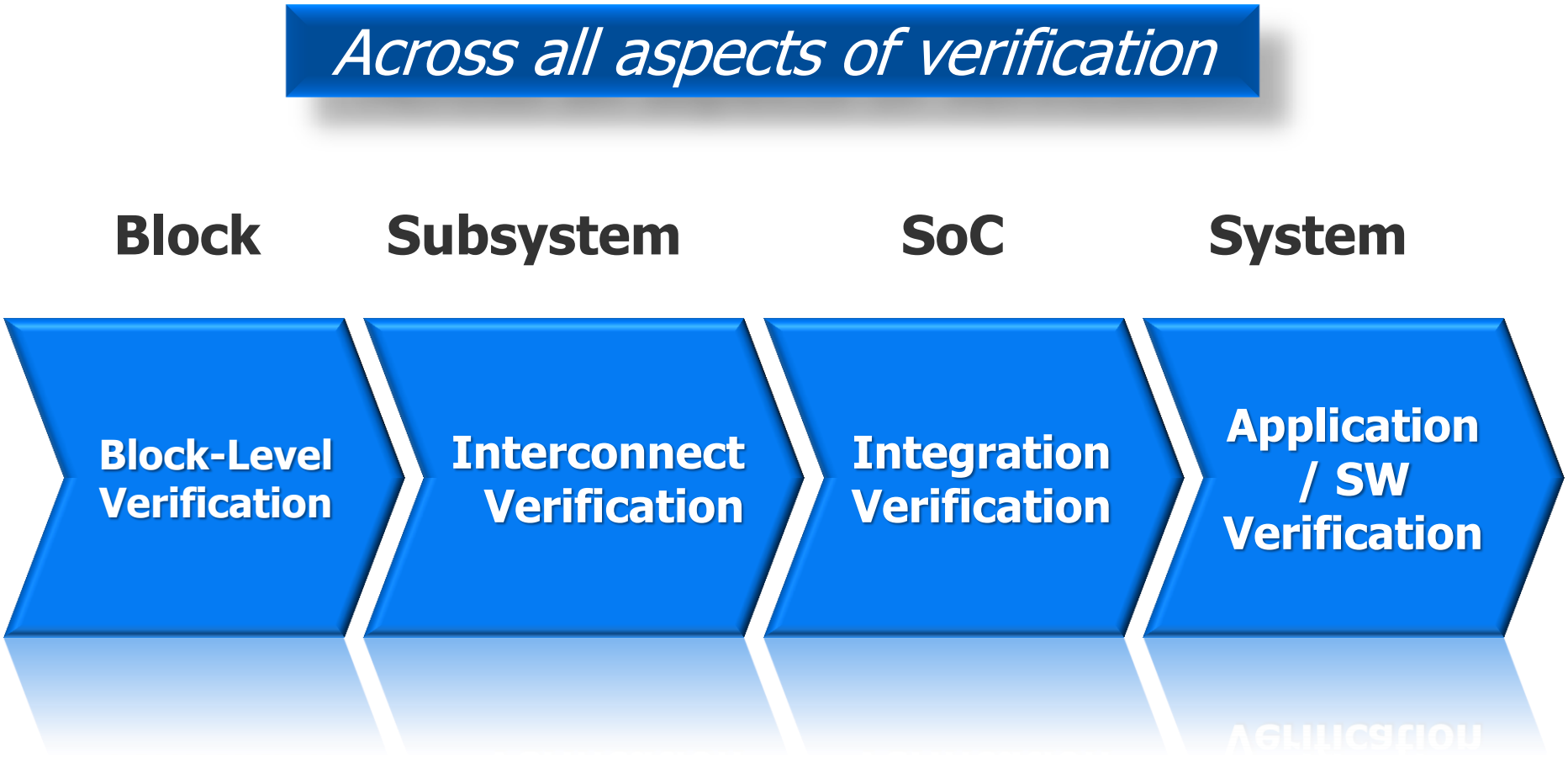

**Adoption by design size for those doing HW acceleration/emulation and FPGA Prototyping**

Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study

# Integrated Simulation/Emulation/Software Verification Environments Emerge

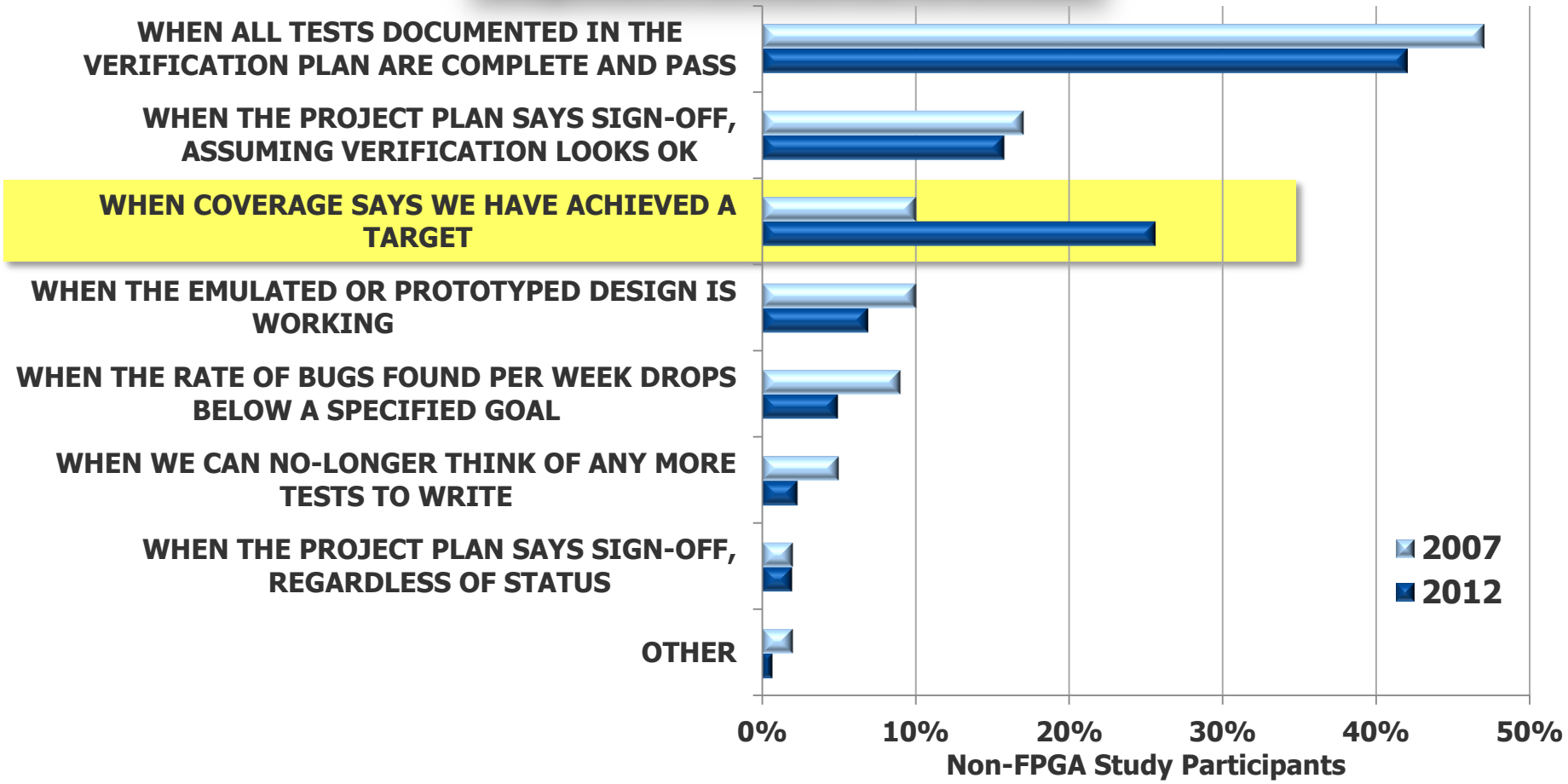
# Coverage and Power

*Across all aspects of verification*



# The Rising Importance of Coverage

## *Signoff criteria trends*

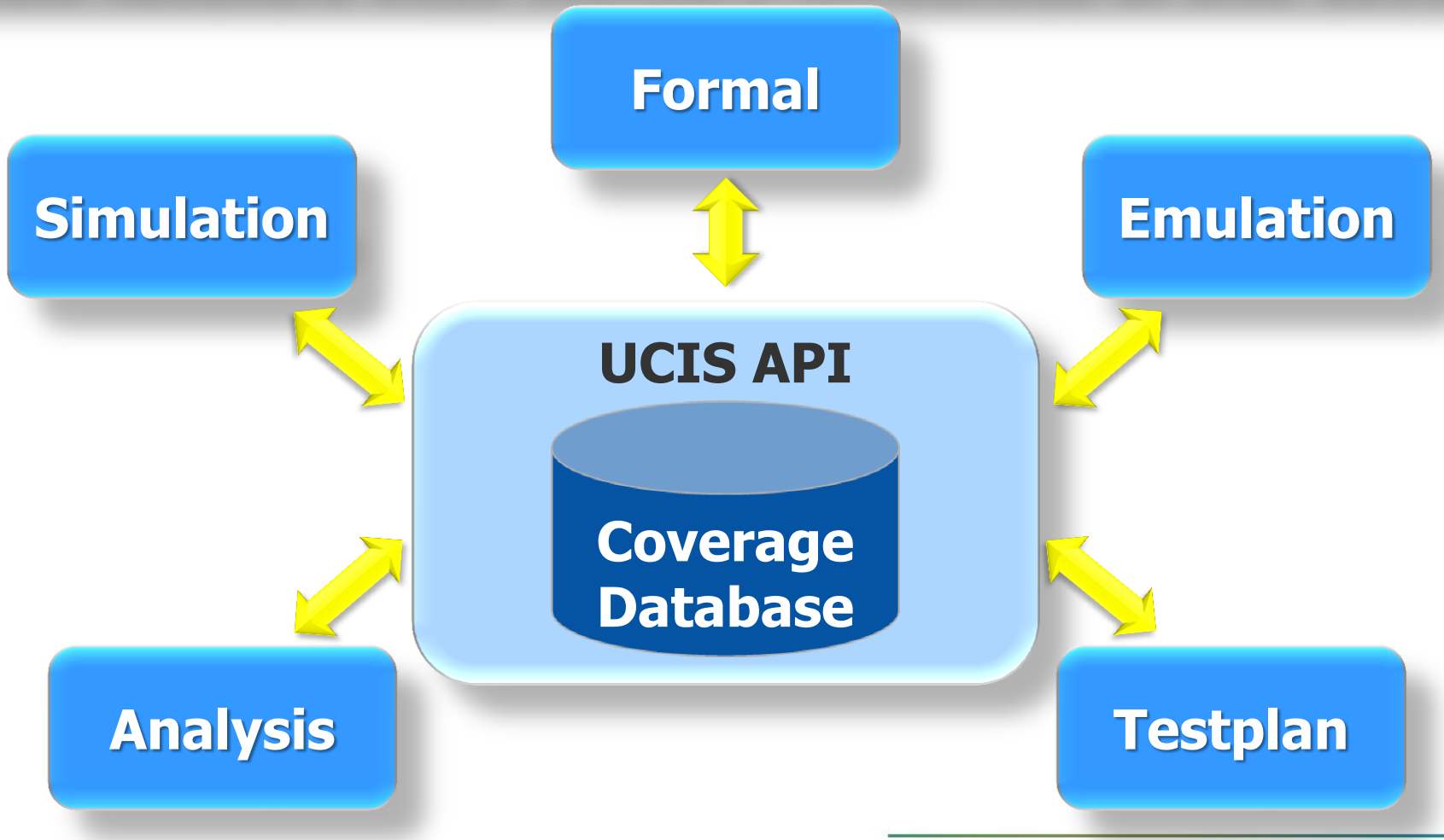



Wilson Research Group and Mentor Graphics, 2012 Functional Verification Study, Used with permission

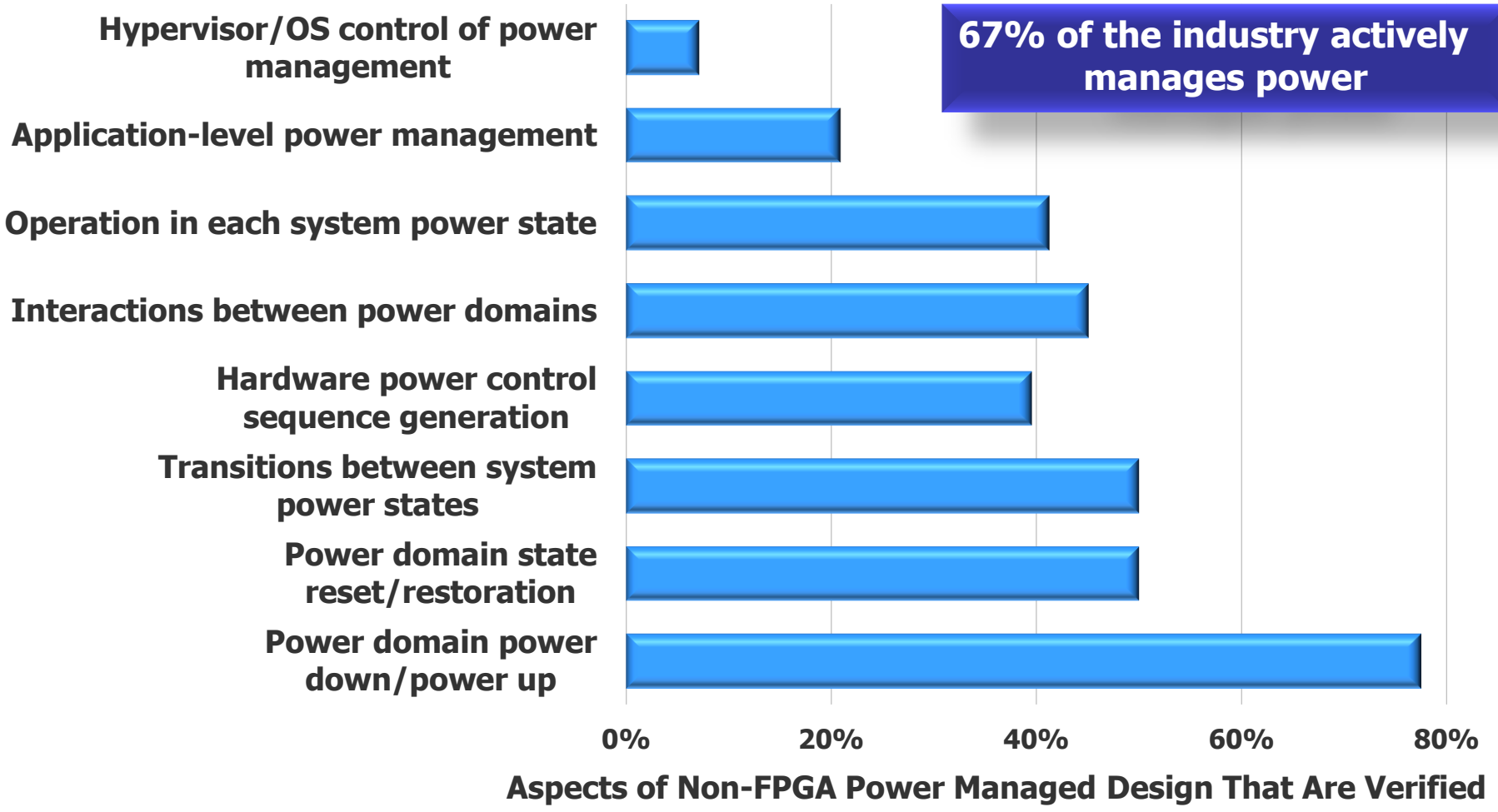
* Multiple answers possible

# Unified Coverage Interoperability Standard

***New Accellera UCIS Standard Announced at DAC 2012***

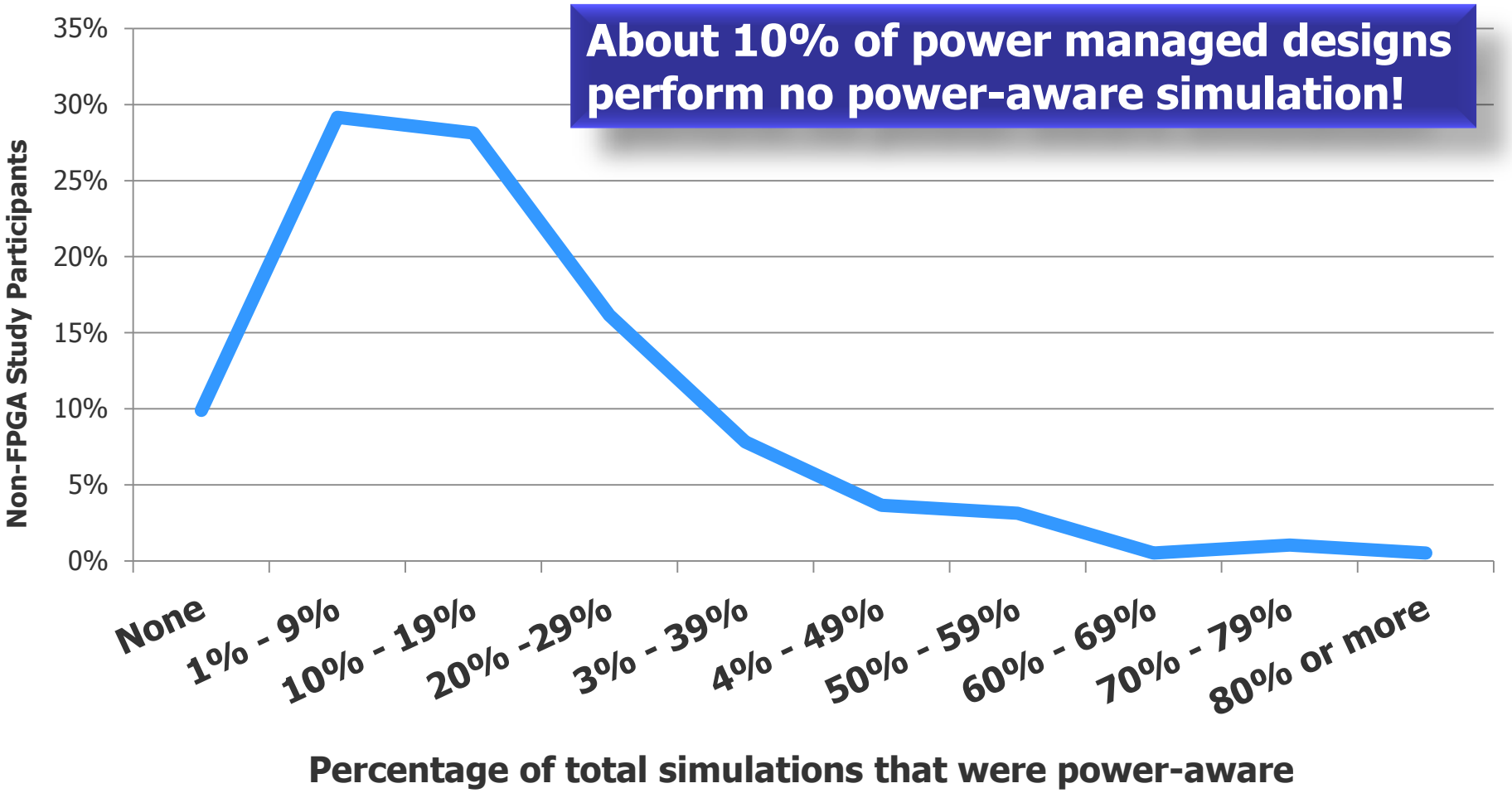


# Trends in Power Management Verification




*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification* Study, Used with permission

# Power Trends

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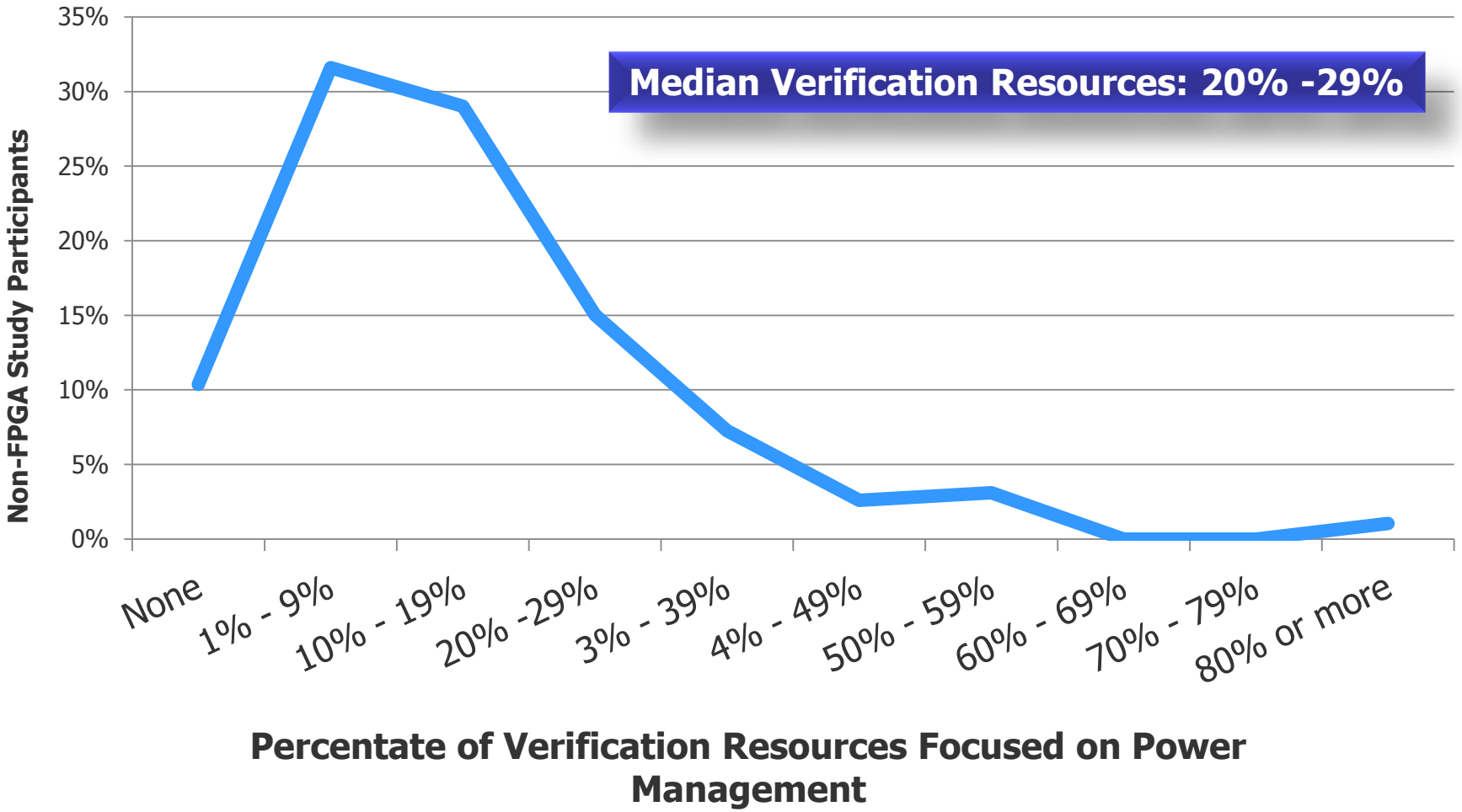
# Power Trends

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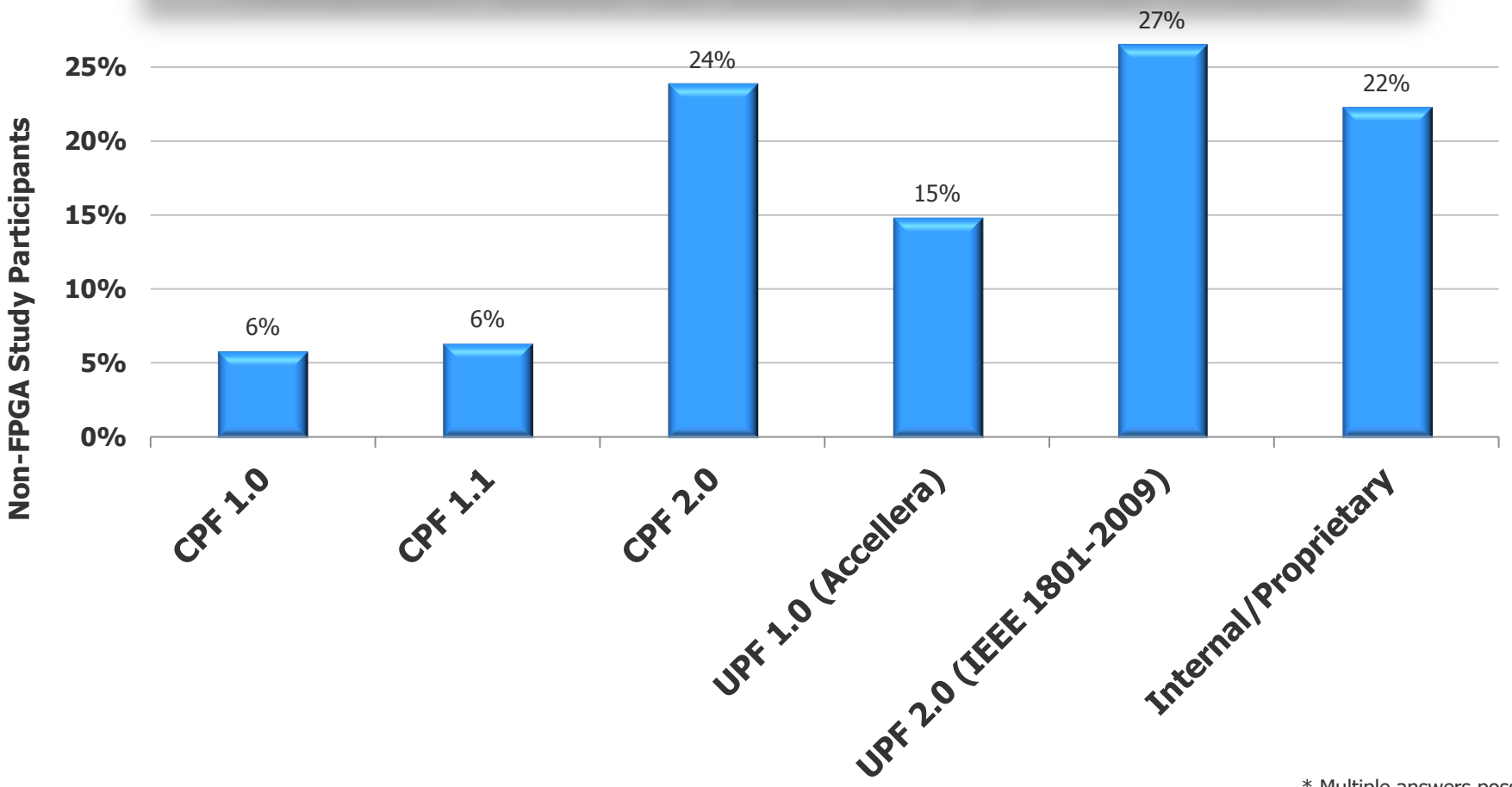
# Power Trends

## *Notation used to describe power intent*

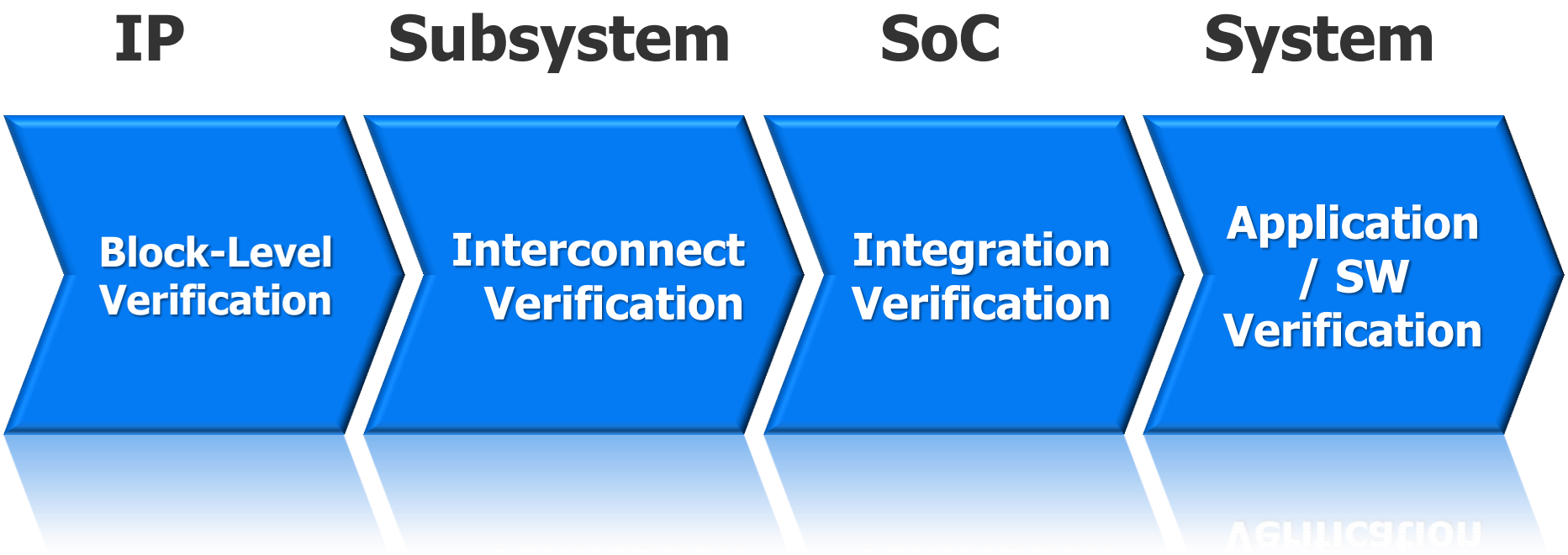



* Multiple answers possible

*Source: Wilson Research Group and Mentor Graphics, 2012 Functional Verification* Study, Used with permission

# Beyond the Status Quo

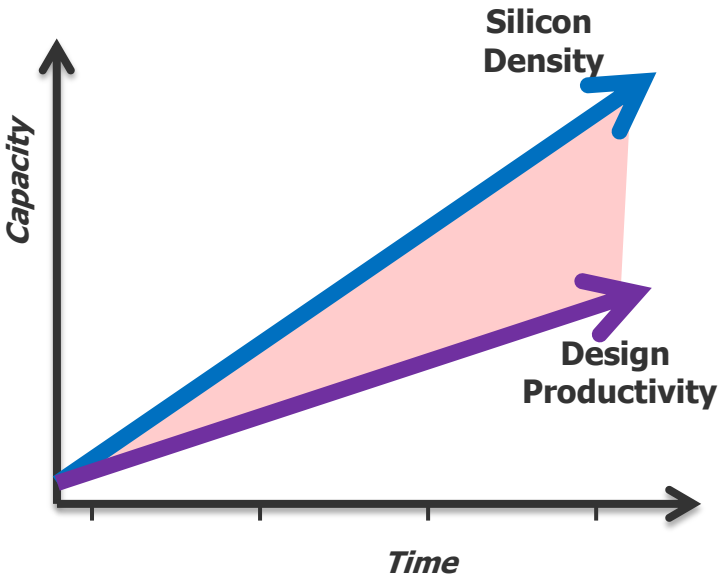
***Standardization of the SoC Verification Process***



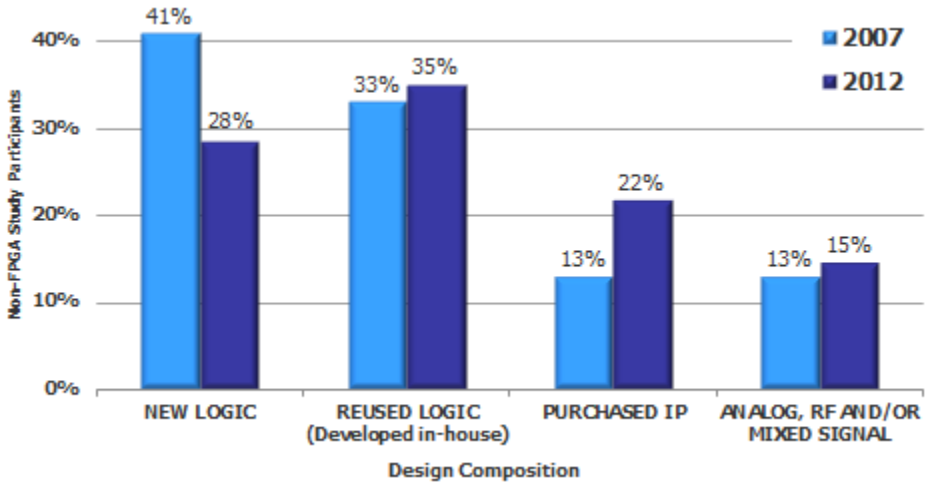
The Productivity Gap

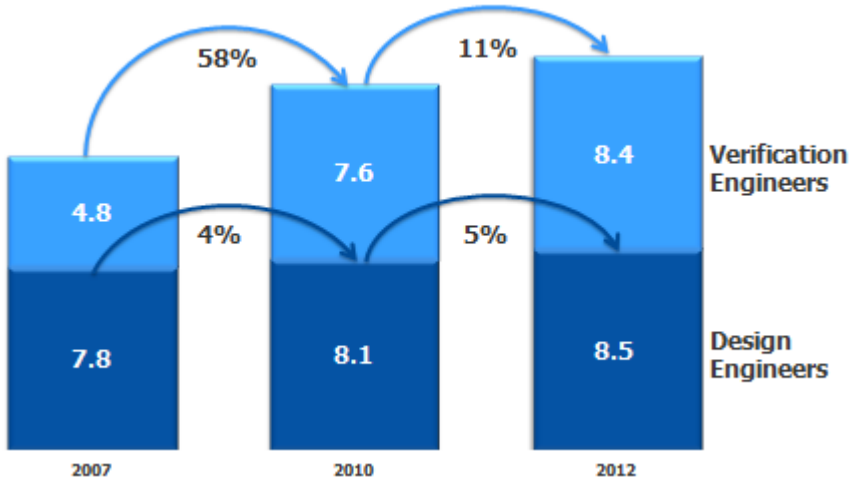
# BACK TO THE FUTURE

# Design Productivity Gap

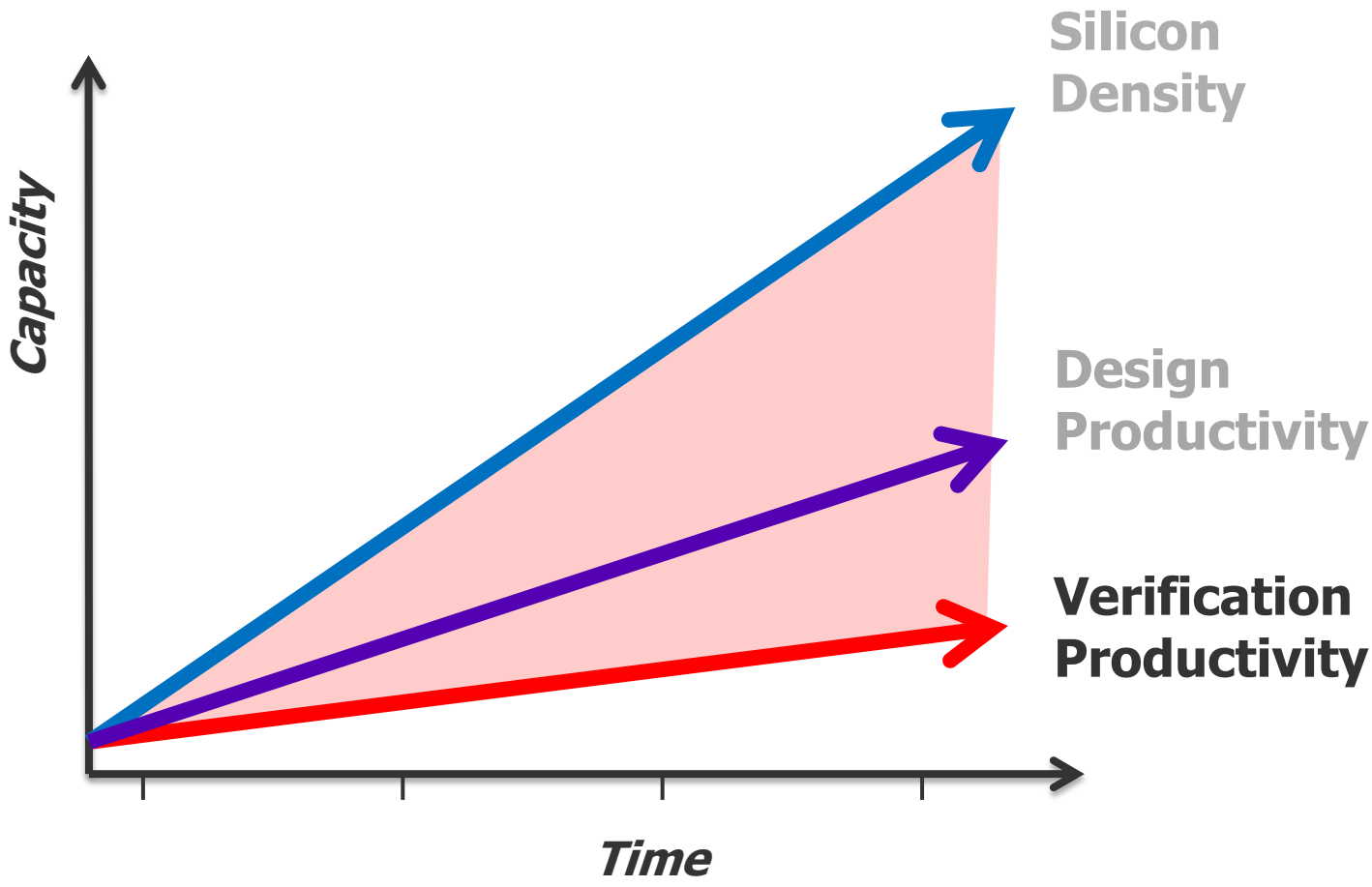



Source: SEMATECH



# Verification Productivity Gap




Source: SEMATECH

# Closing The Verification Gap

Reuse

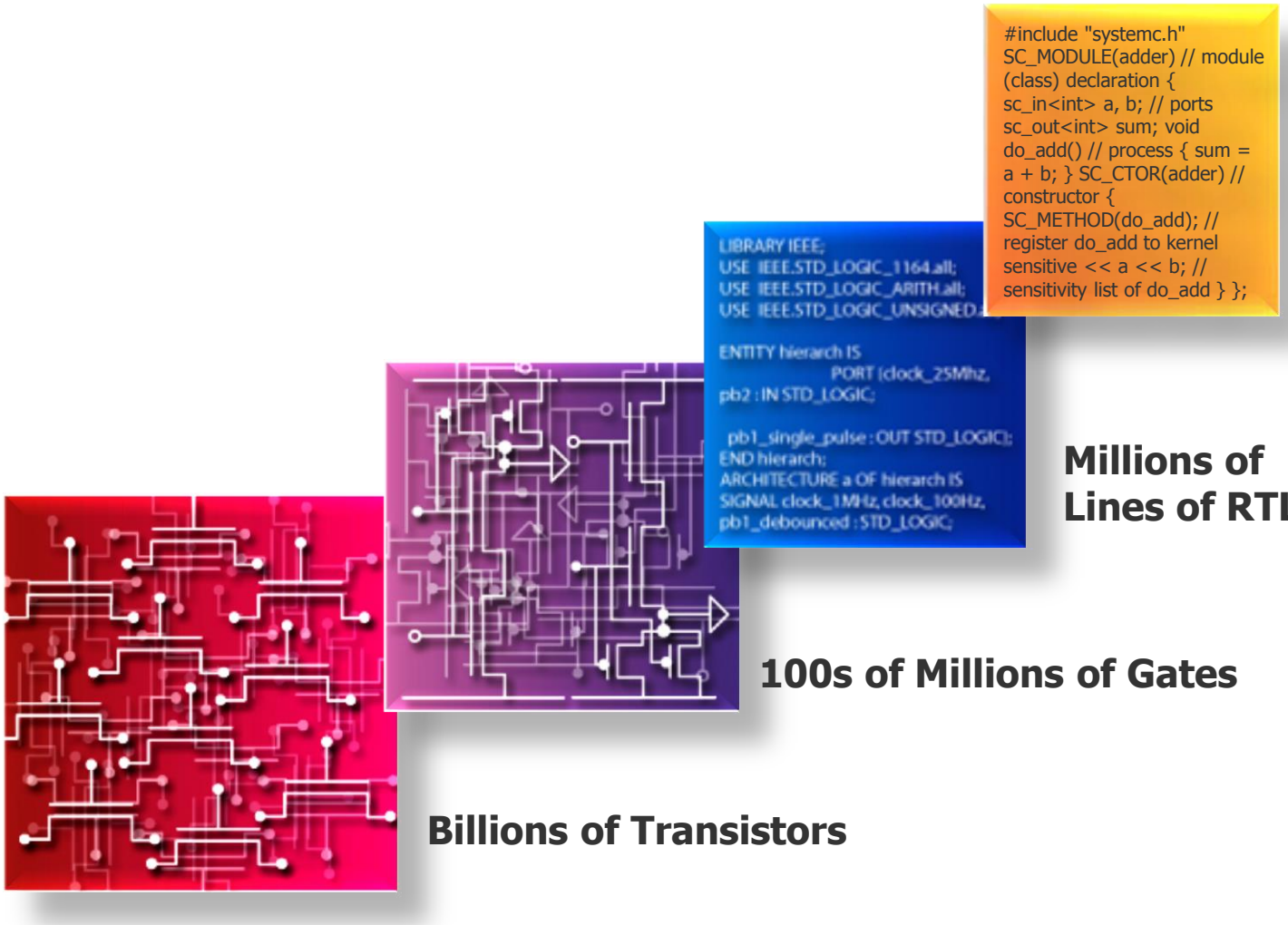
Abstraction

?

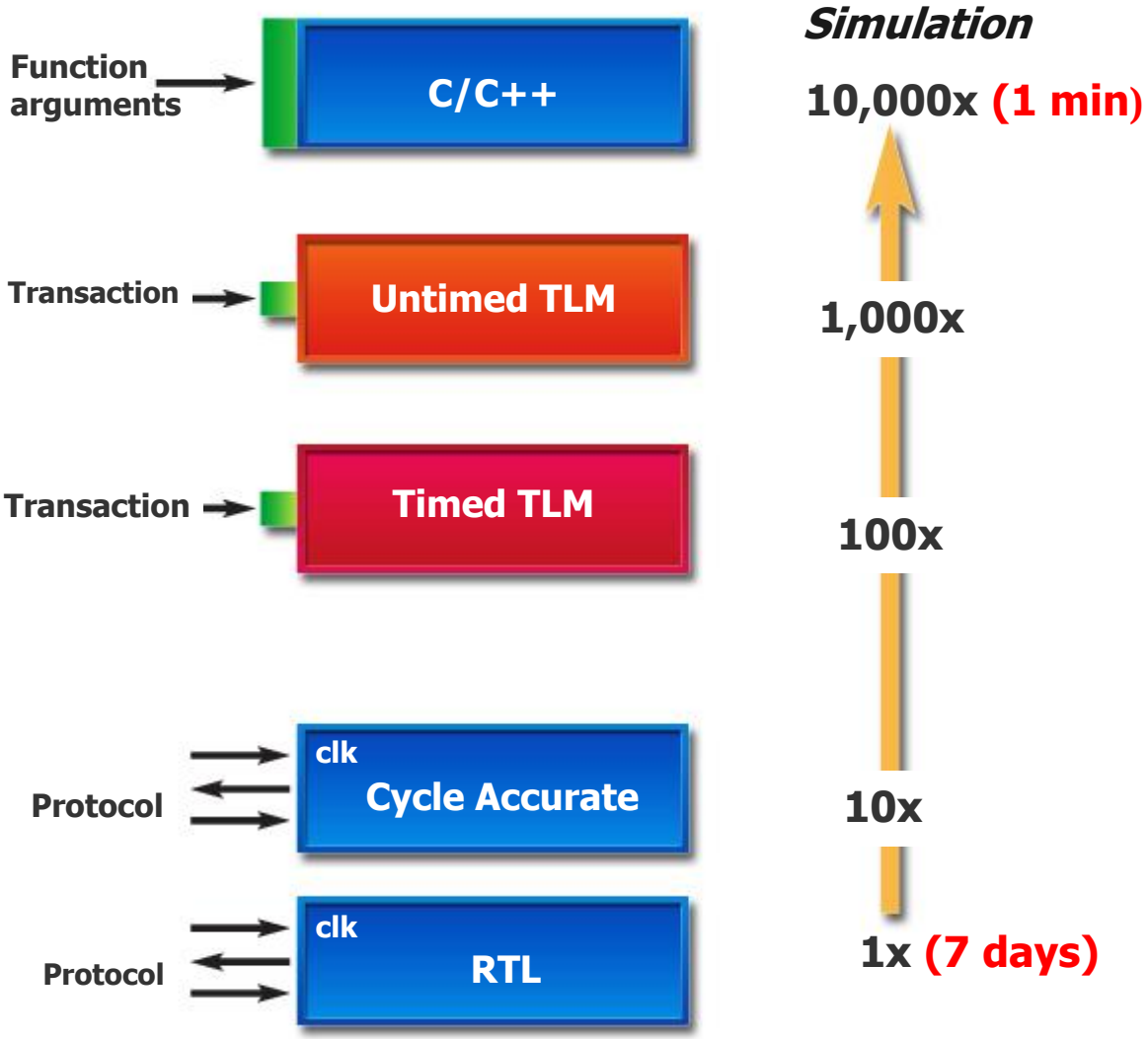
Acceleration

Methodology

# Managing Complexity



# Productivity Gains Through Abstraction



# Bug Prevention vs. Bug Hunting

***What's the advantage of SystemC compared with RTL?***

**There are two different aspects – quality and time schedule. Today, a full chip on SystemC will run around 10 MHz, and you will never reach that speed using RTL or a lower-level abstraction. It's similar to a prototype speedup. Previously with RTL designs, our bug rate was in the range of 10 to 50 bugs per square millimeter. Now we are at less than one bug per millimeter squared. So we have both quality and speed of development.**

Source: EETimes, 2007, Laurent Ducousso, who manages intellectual-property (IP) verification for STMicroelectronics' Home Entertainment Division

# Summary

- Beyond theory in terms of rising complexity
- Beyond arguing over who won the standards wars
- Beyond surviving by maintaining the status quo

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