Equivalence Checking For Synchronous Elastic Circuits

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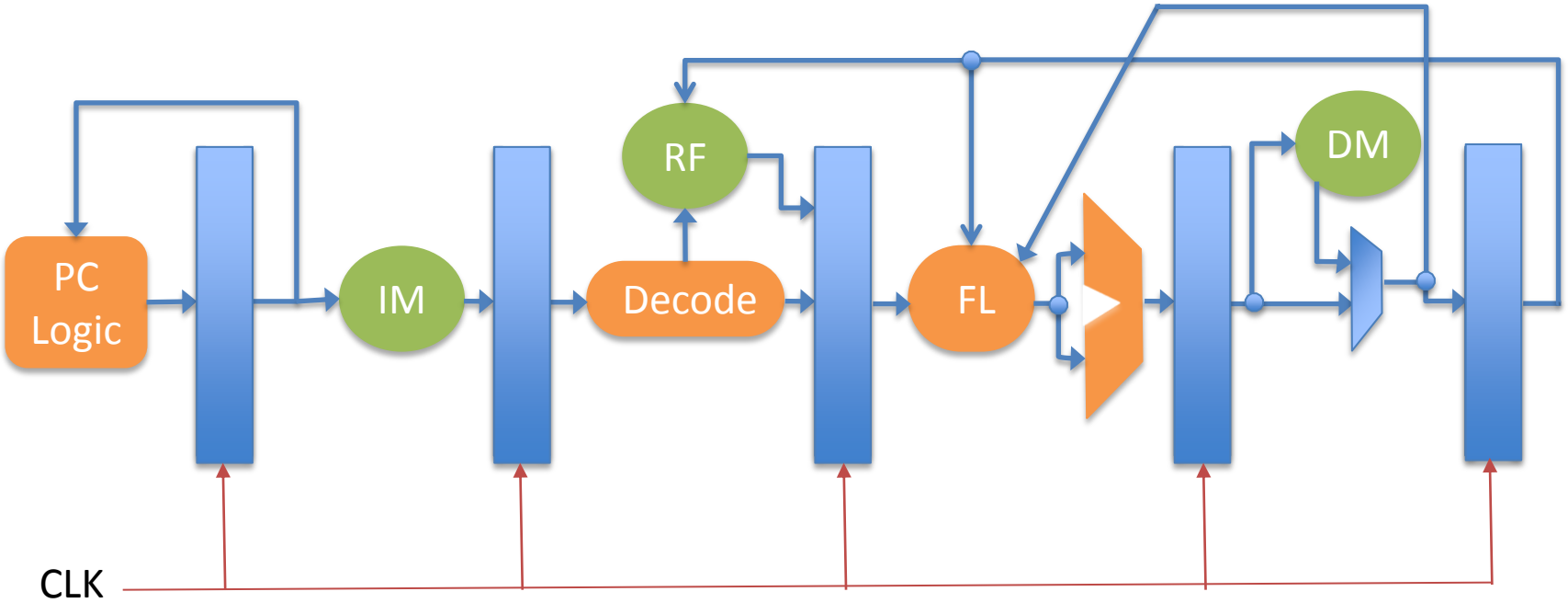
Synchronous elastic circuits

- Clock-based latency insensitive circuits
- Advantages:
  - Provides a solution to wire-delay challenge
  - Use of existing EDA CAD flows
  - IP reuse in SOC design

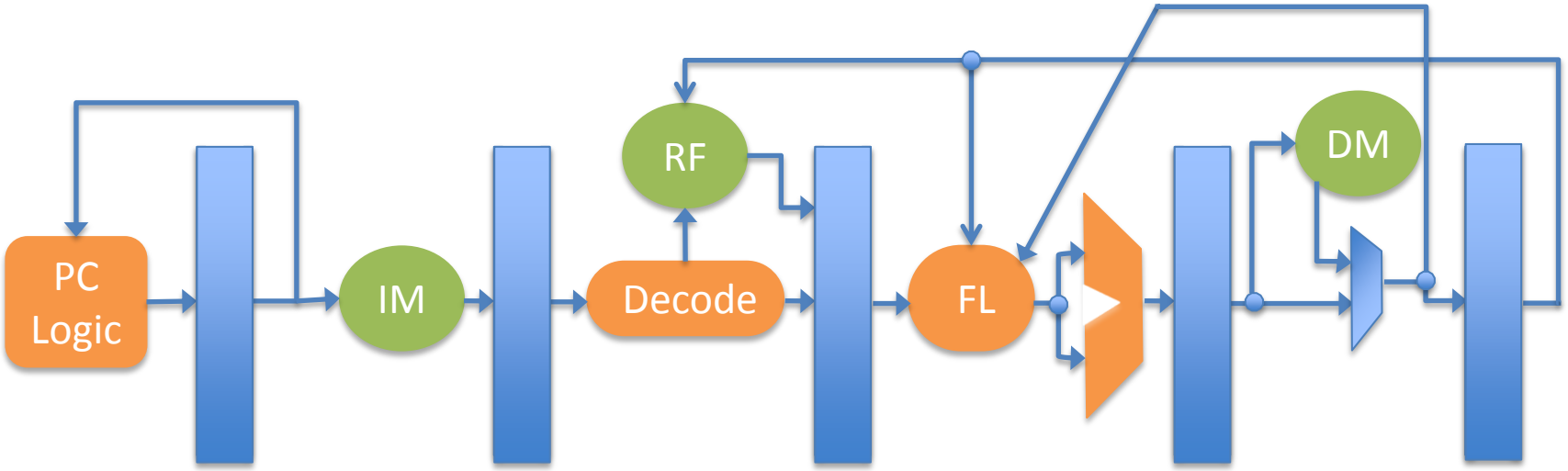
Synchronous elastic circuits

- Latency insensitive protocols
  - Carloni et al. (*CAV 1999*)
- Theory of latency-insensitive design
  - Carloni et al. (*IEEE TCAD 2001*)
- Coping with latency in soc design
  - Carloni et al. (*IEEE Micro 2002*)
- Synthesis of synchronous elastic architectures
  - Cortadella et al. (*DAC 2006*)

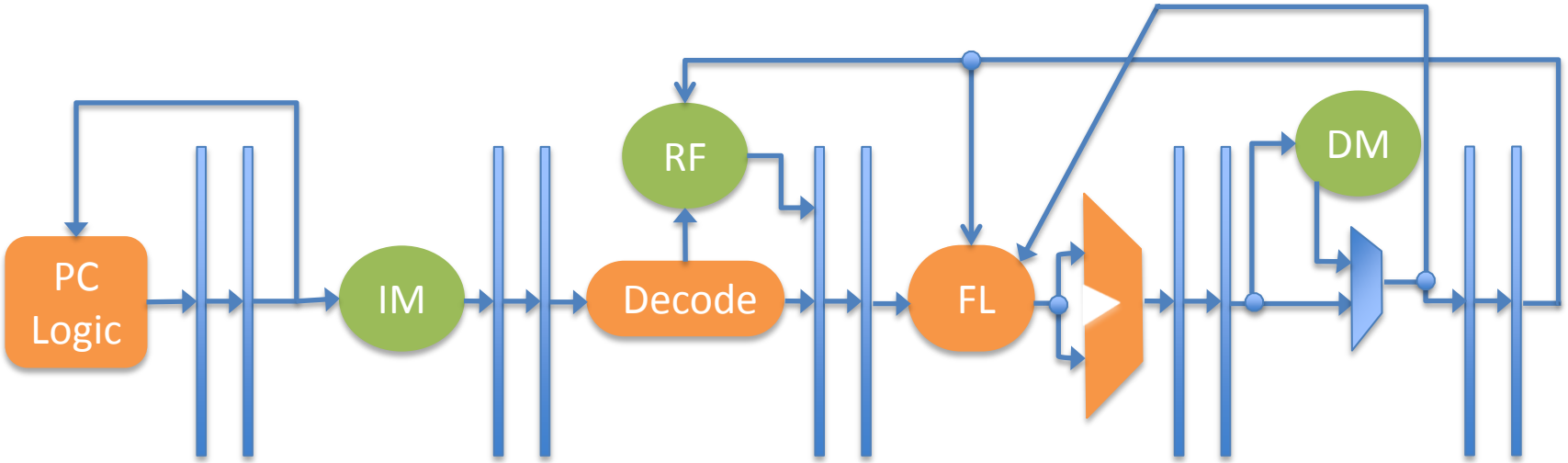
Elasticization



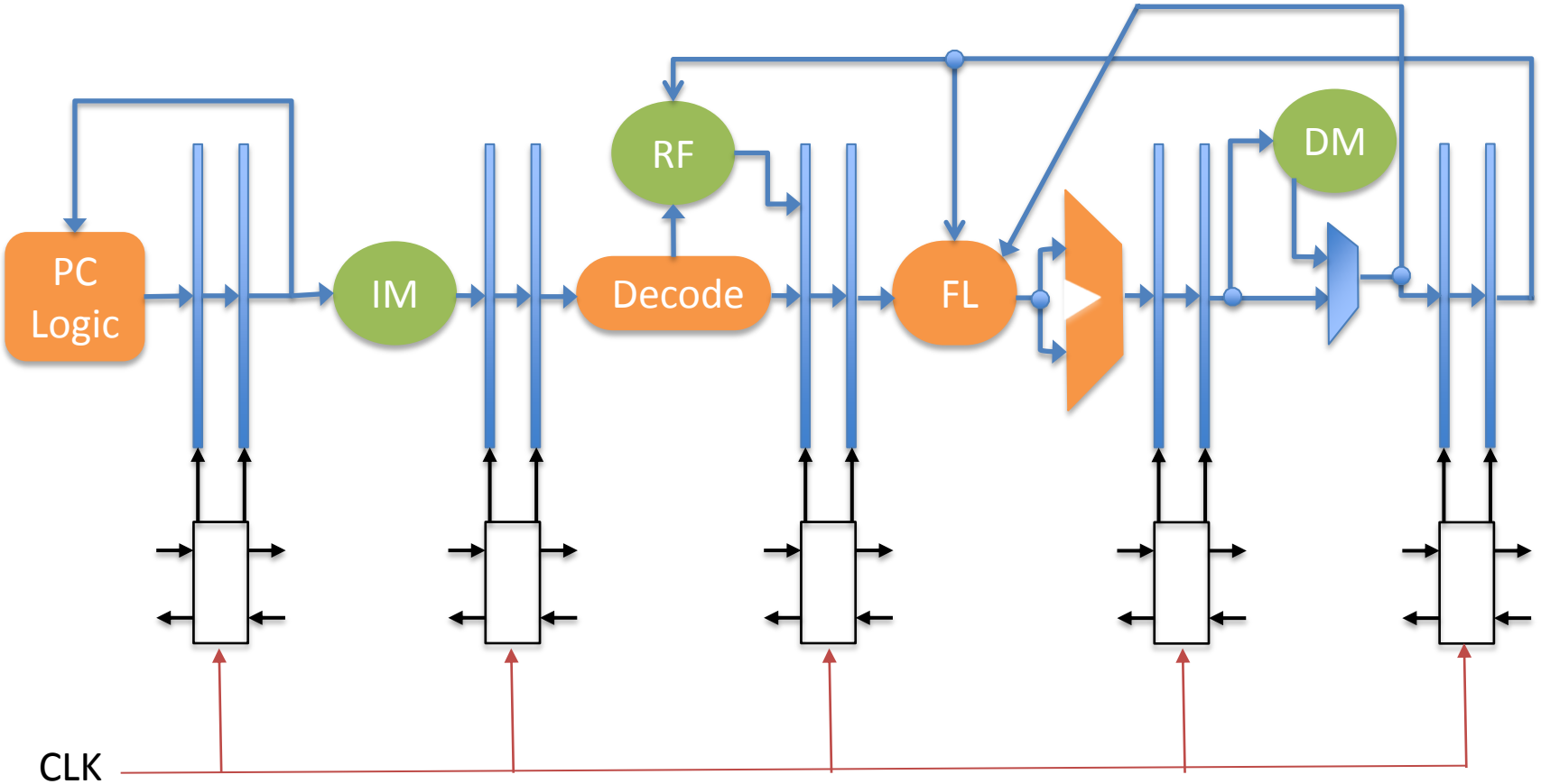
Elasticization



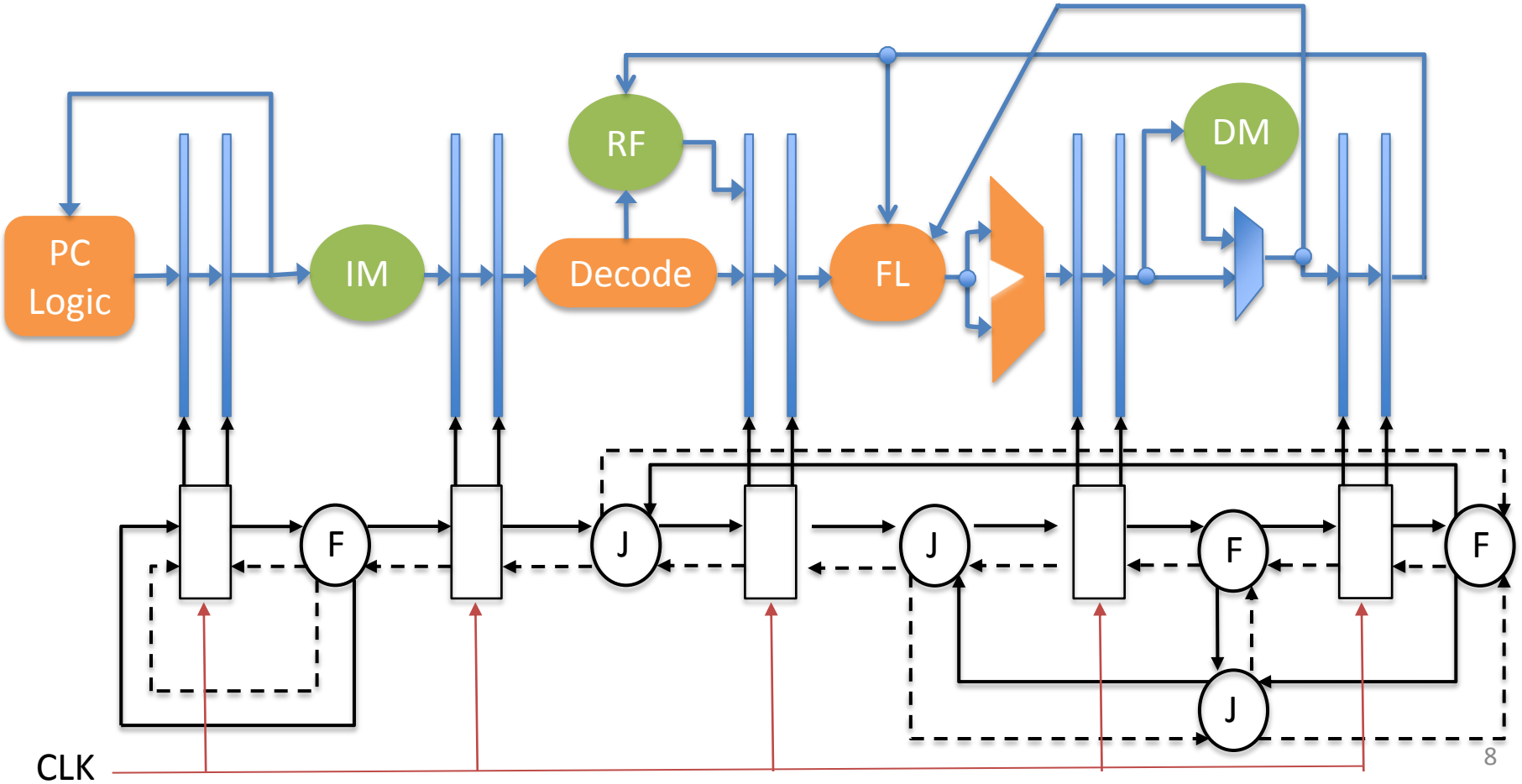
Elasticization



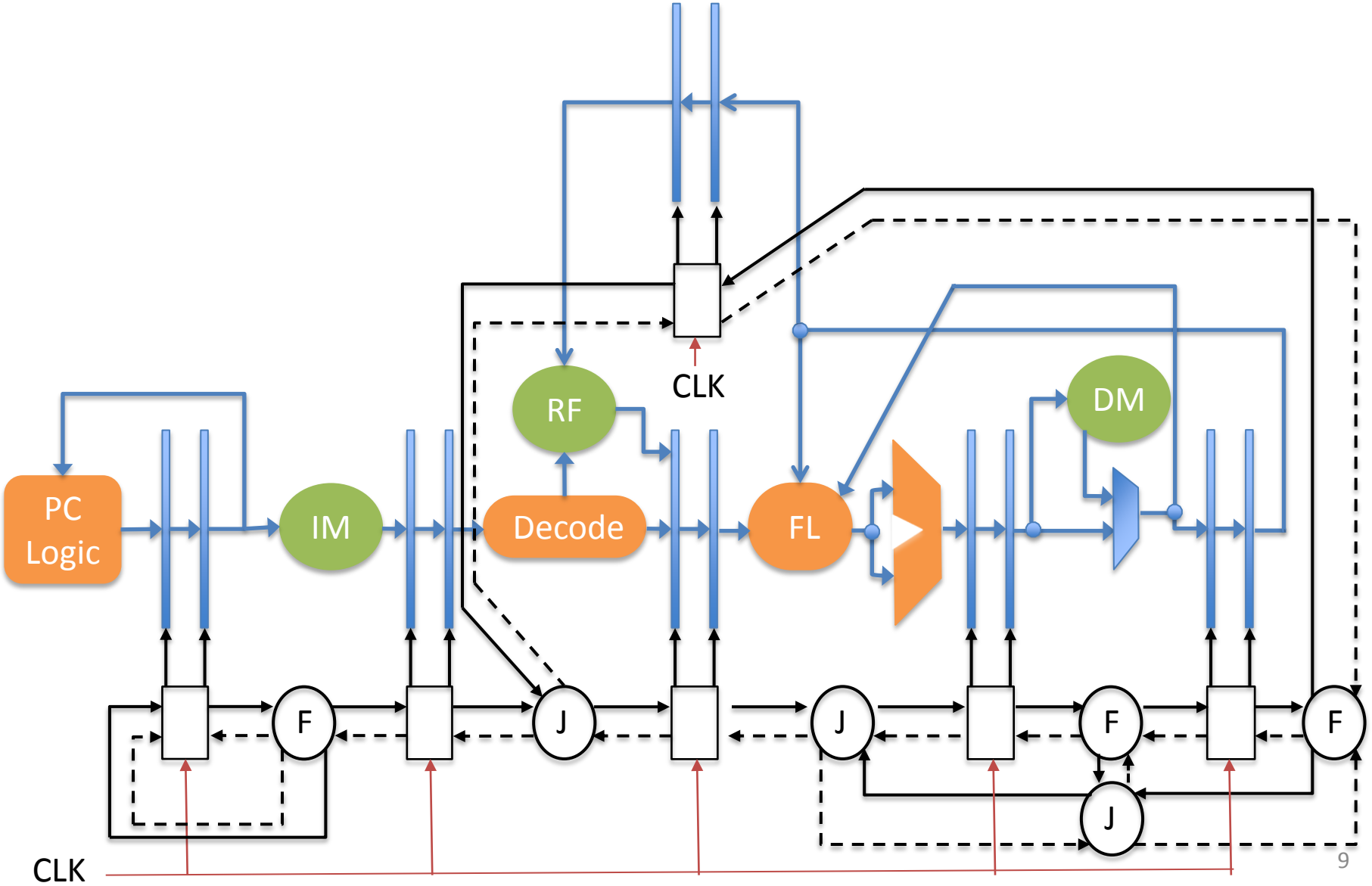
Elasticization

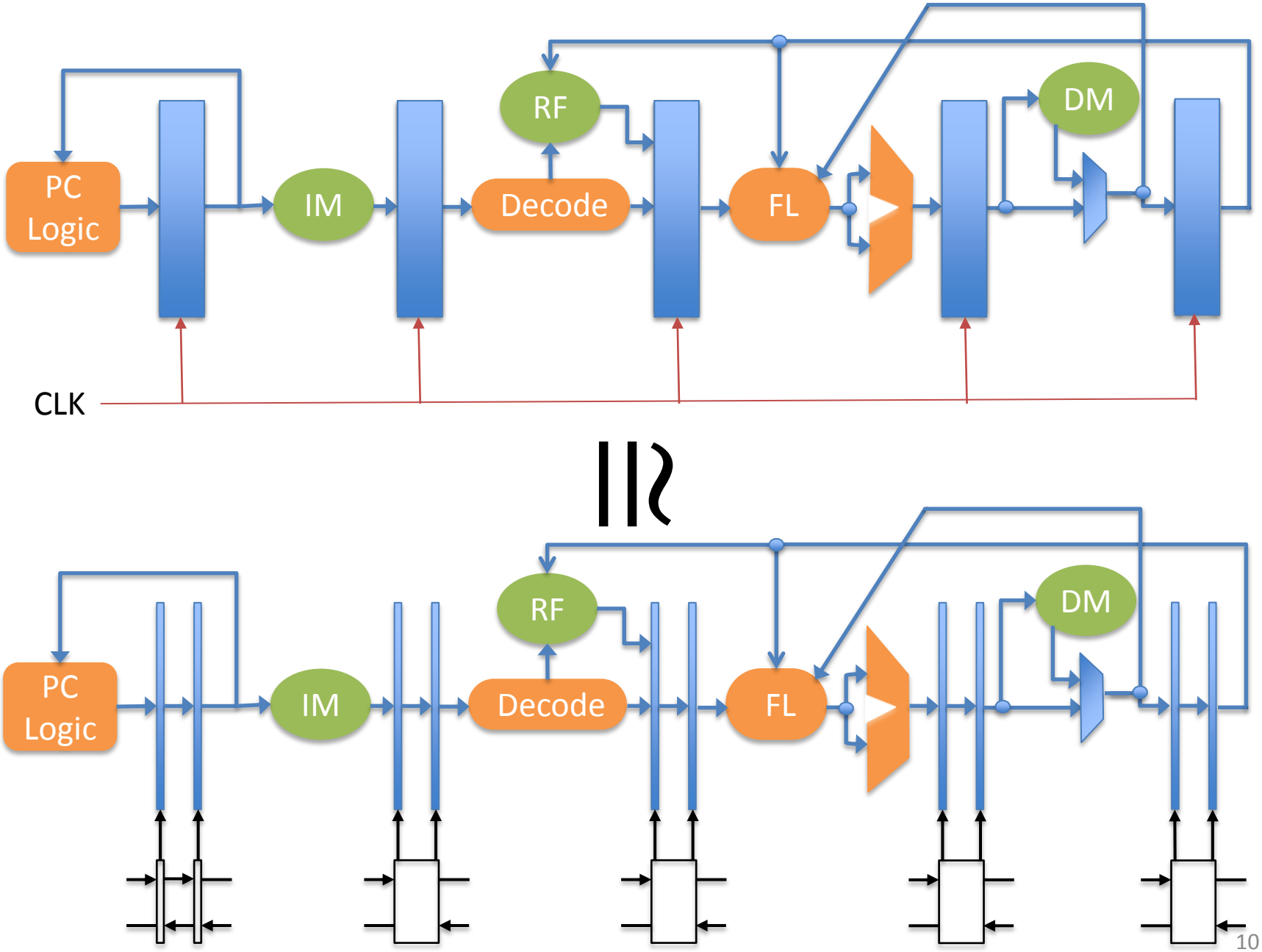


Elasticization



Resolve timing issues




PC Logic
IM
RF
Decode
FL
DM
CLK
PC Logic
IM
RF
Decode
FL
DM

Equivalence Verification

- Well Founded Equivalence Bisimulations (WEBs) Refinement
  - Panagiotis (Pete) Manolios: Correctness of Pipelined Machines (FMCAD'00)
- Stuttering
- Refinement Map
- Rank functions

WEB Refinement Formula

- w : Implementation State
- s = *refinement-map*(w)
- v = *implementation-step*(w)
- u = *specification-step*(s)

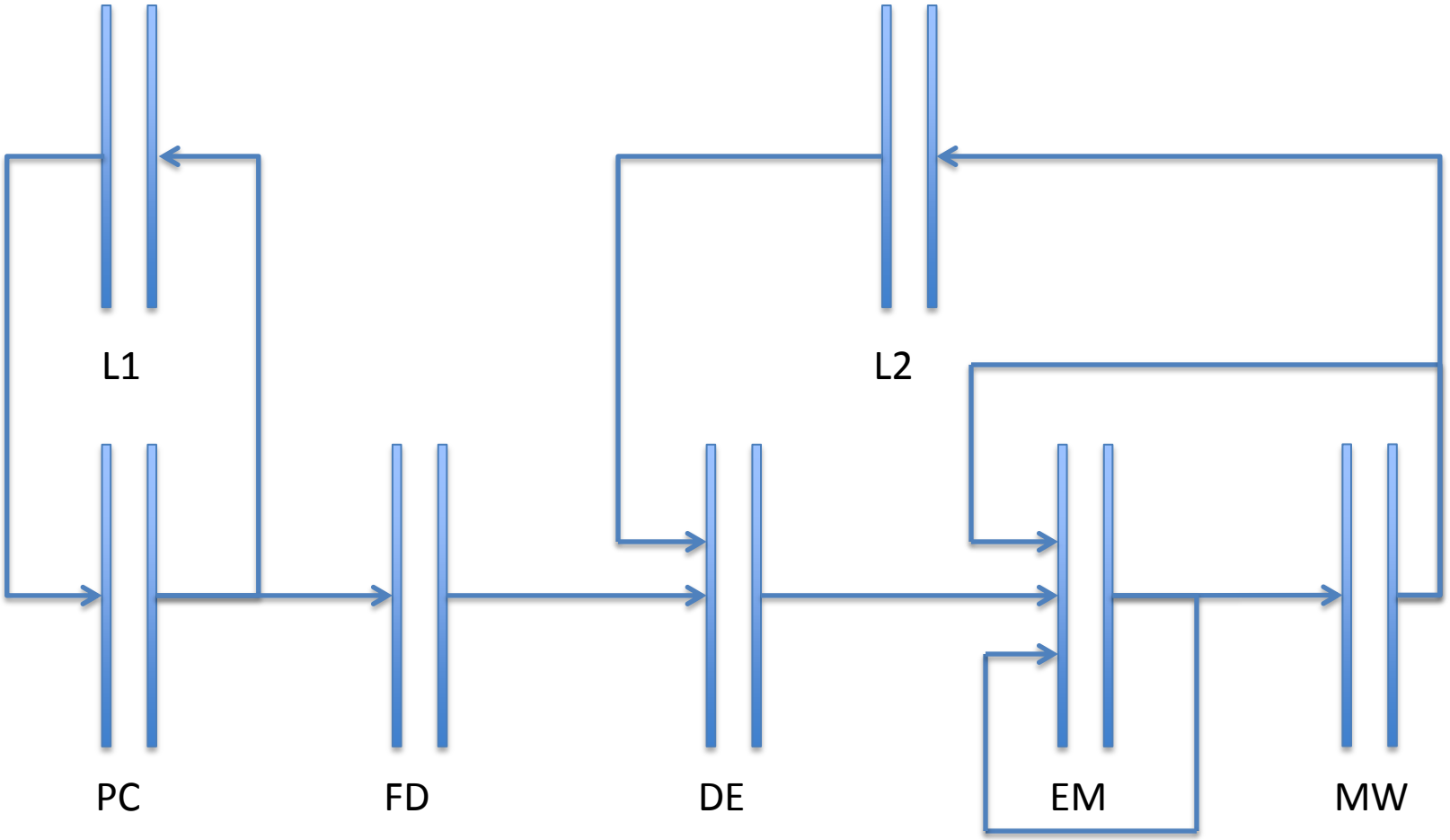
$\forall w \in$ IMPL ::

1. u = *refinement-map*(v) {non-stuttering step}
2. s = *refinement-map*(v) $\wedge$
   rank(v) < *rank*(w) {stuttering step}

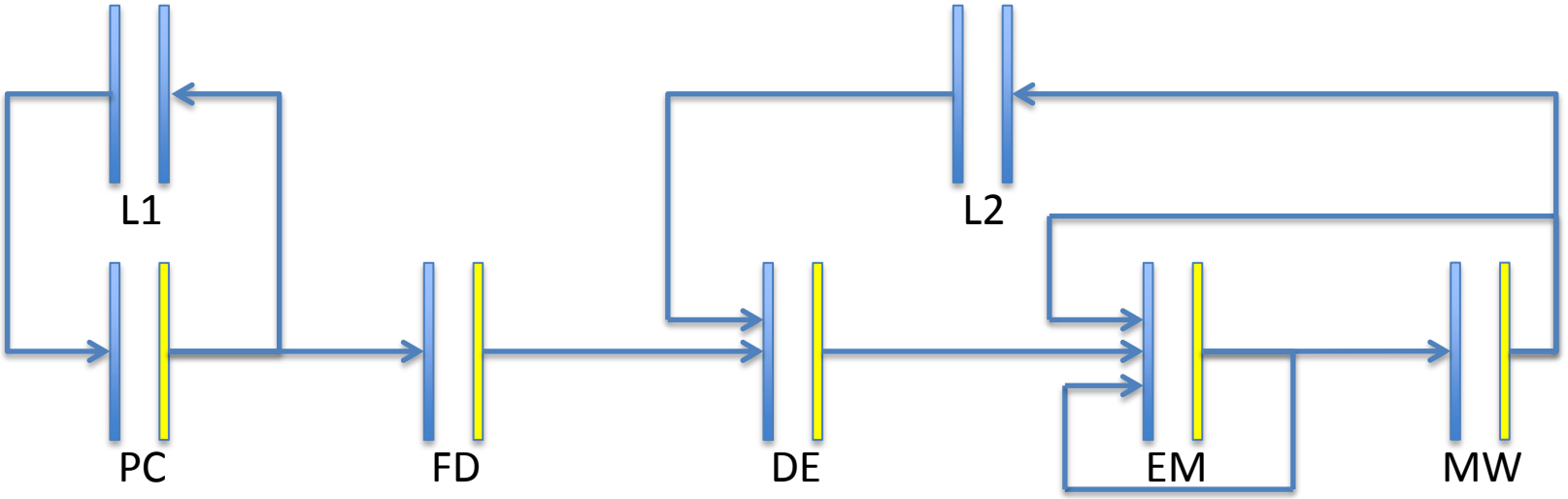
Equivalence Verification

- Synchronous Pipeline
  - Pipeline registers
  - D Flip Flops
  - Stages synchronized
- Synchronous Elastic Pipeline
  - Elastic buffers
  - Additional elastic buffers arbitrarily inserted to break wire delays
  - Elastic controller network layer between the clock and the pipeline
  - Stages not synchronized

Reachability Analysis

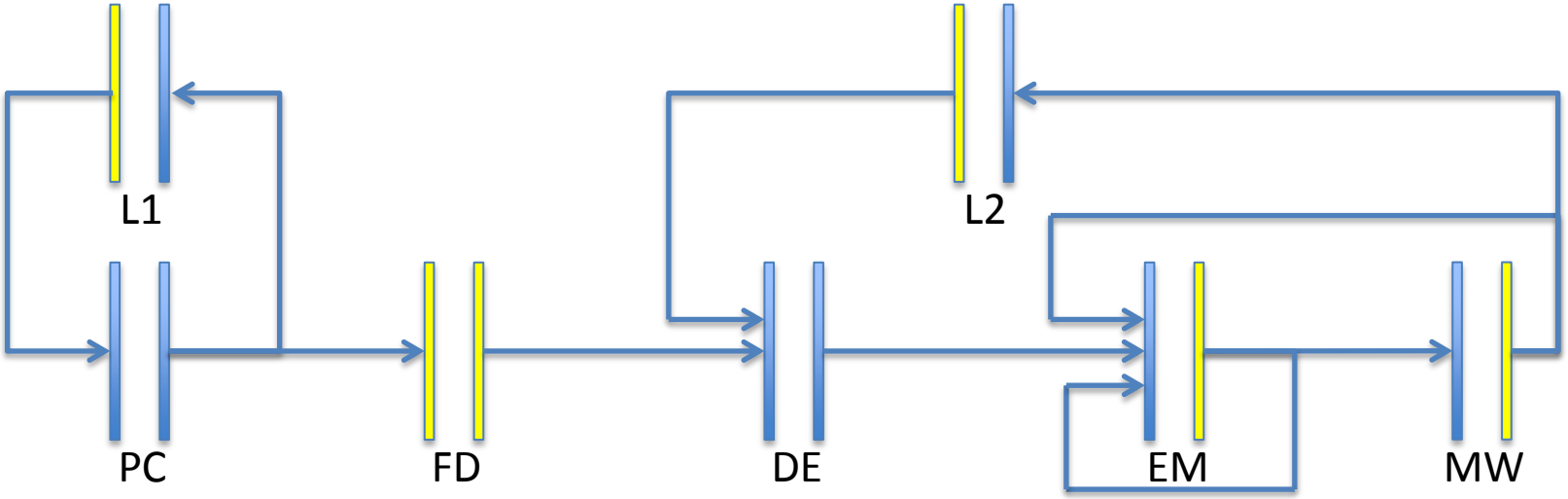


Reachability Analysis



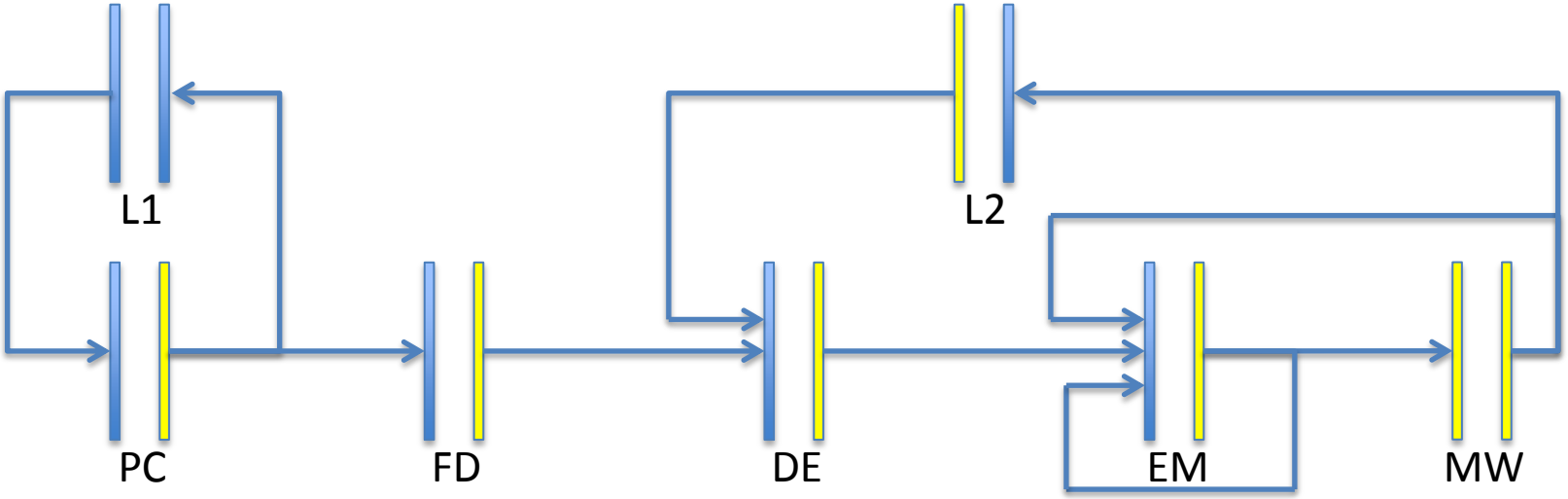
State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0

Reachability Analysis



State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0
1	0	0	1	2	0	0	0	6	0	4	0	1	0	5

Reachability Analysis



State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0
1	0	0	1	2	0	0	0	6	0	4	0	1	0	5
2	0	7	0	1	0	8	0	6	6	4	0	0	0	4

Reachability Analysis

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0
1	0	0	1	2	0	0	0	6	0	4	0	1	0	5
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16

Eventually converges

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0
1	0	0	1	2	0	0	0	6	0	4	0	1	0	5
2	0	7	0	1	0	8	0	6	6	4	0	0	0	4
3	0	0	0	7	0	9	0	10	0	6	0	7	0	0
4	0	11	0	7	0	0	0	12	0	10	0	0	0	6
5	0	0	0	11	0	13	0	12	12	10	0	0	0	6
6	0	14	0	0	0	15	0	16	0	12	0	0	0	0
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0
1	0	0	1	2	0	0	0	6	0	4	0	1	0	5
2	0	7	0	1	0	8	0	6	6	4	0	0	0	4
3	0	0	0	7	0	9	0	10	0	6	0	7	0	0
4	0	11	0	7	0	0	0	12	0	10	0	0	0	6
5	0	0	0	11	0	13	0	12	12	10	0	0	0	6
6	0	14	0	0	0	15	0	16	0	12	0	0	0	0
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
0	0	1	0	2	0	3	0	4	0	5	0	0	0	0
1	0	0	1	2	0	0	0	6	0	4	0	1	0	5
2	0	7	0	1	0	8	0	6	6	4	0	0	0	4
3	0	0	0	7	0	9	0	10	0	6	0	7	0	0
4	0	11	0	7	0	0	0	12	0	10	0	0	0	6
5	0	0	0	11	0	13	0	12	12	10	0	0	0	6
6	0	14	0	0	0	15	0	16	0	12	0	0	0	0
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16

Refinement map computation

State	PC	FD	DE	EM	MW
0	1	2	3	4	5
1	7	1	8	6	4
2	11	7	9	10	6
3	14	11	13	12	10
4	18	14	15	16	12

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16
10	0	21	0	0	0	22	0	20	20	17	0	0	0	17
11	0	0	0	21	0	0	0	23	0	20	0	21	0	17
12	0	24	0	0	0	25	0	23	23	20	0	0	0	20
13	0	0	0	24	0	0	0	26	0	23	0	24	0	20

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16
10	0	21	0	0	0	22	0	20	20	17	0	0	0	17
11	0	0	0	21	0	0	0	23	0	20	0	21	0	17
12	0	24	0	0	0	25	0	23	23	20	0	0	0	20
13	0	0	0	24	0	0	0	26	0	23	0	24	0	20

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16
10	0	21	0	0	0	22	0	20	20	17	0	0	0	17
11	0	0	0	21	0	0	0	23	0	20	0	21	0	17
12	0	24	0	0	0	25	0	23	23	20	0	0	0	20
13	0	0	0	24	0	0	0	26	0	23	0	24	0	20

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16
10	0	21	0	0	0	22	0	20	20	17	0	0	0	17
11	0	0	0	21	0	0	0	23	0	20	0	21	0	17
12	0	24	0	0	0	25	0	23	23	20	0	0	0	20
13	0	0	0	24	0	0	0	26	0	23	0	24	0	20

21	18	19	17	16

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16
10	0	21	0	0	0	22	0	20	20	17	0	0	0	17
11	0	0	0	21	0	0	0	23	0	20	0	21	0	17
12	0	24	0	0	0	25	0	23	23	20	0	0	0	20
13	0	0	0	24	0	0	0	26	0	23	0	24	0	20

21	18	19	17	16

Refinement map computation

State	PC		FD		DE		EM		MW		L1		L2	
	m	s	m	s	m	s	m	s	m	s	m	s	m	s
7	0	0	0	14	0	0	0	17	0	16	0	14	0	12
8	0	18	0	0	0	19	0	17	17	16	0	0	0	16
9	0	0	0	18	0	0	0	20	0	17	0	18	0	16
10	0	21	0	0	0	22	0	20	20	17	0	0	0	17
11	0	0	0	21	0	0	0	23	0	20	0	21	0	17
12	0	24	0	0	0	25	0	23	23	20	0	0	0	20
13	0	0	0	24	0	0	0	26	0	23	0	24	0	20

	PC	FD	DE	EM	MW
History	-1	-2	-3	-3	-3

Verification Tool

- Verific front end parser
- Metadata of the circuit structure
- Translated to SMT (QF_ABV)
- Verification performed using Z3 decision procedure (version 4.3.0)

Elastic Models

- E-n-0 : 0 additional buffers, n bit datapath
- E-n-1 : 1 additional buffers, n bit datapath
- E-n-2 : 2 additional buffers, n bit datapath
- E-n-3 : 3 additional buffers, n bit datapath
- E-n-4 : 4 additional buffers, n bit datapath
- E-n-5 : 5 additional buffers, n bit datapath
- EB1-n-2: Buggy E-n-2 (datapath bug)
- EB1-n-2: Buggy E-n-2 (controlpath bug)

  (n = 32, 64, 128)

Verification Results

Benchmark	No. of gates	No. of latches	Time for generation of proof obligations (sec)	SMT statistics	
				Time (sec)	Memory (kB)
E-128-0	494,171	2,156	3.972	560.88	588.13
E-128-1	495,481	2,416	5.388	764.72	157.77
E-128-2	496,851	2,688	5.568	947.30	313.51
E-128-3	498,221	2,960	5.488	445.12	341.87
E-128-4	499,591	3,232	5.680	792.69	240.52
E-128-5	500,961	3,504	5.788	606.68	237.73
EB1-128-2	496,840	2,688	5.420	273.84	158.45
EB2-128-2	496,851	2,688	5.516	14.46	156.73

Conclusions

- The tool was able to handle benchmarks that has over 0.5 **M** gates and over 3,500 latches.
- Sequential equivalence checking using refinement by automatically synthesizing the refinement maps.

Future Work

- Extend to deal with open networks with non-deterministic behavior
- Explore for other latency insensitive design paradigms

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